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Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems

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ABSTRACT

The assembly of nanowires and nanotubes into arrays patterned on multiple length scales is critical to the realization of integrated electronic and photonic nanotechnologies. A general and efficient solution-based method for controlling organization and hierarchy of nanowire structures over large areas has been developed. Nanowires were aligned with controlled nanometer to micrometer scale pitch using the Langmuir–Blodgett technique and transferred to planar substrates in a layer-by-layer process to form parallel and crossed nanowire structures. The parallel and crossed nanowire structures were efficiently patterned into repeating arrays of controlled dimensions and pitch using photolithography to yield hierarchical structures with order defined from the nanometer through centimeter length scales. In addition, electrical transport studies show that reliable electrical contacts can be made to the hierarchical nanowire arrays prepared by this method. This solution-based process offers a flexible pathway for bottom-up assembly of virtually any nanowire material into highly integrated and hierarchically organized nanodevices needed for a broad range of functional nanosystems.

Semiconductor nanowires (NWs) and carbon nanotubes represent promising building blocks for the bottom-up assembly of integrated electronic and photonic systems because these materials can exhibit diverse device behavior and simultaneously function as the ‘wires’ that access and interconnect devices.[1−3] Efforts to date have focused primarily on the demonstration of individual nanodevices including field effect transistors,[4−7] diodes,[8,9] light-emitting diodes,[6,9,10] and diode lasers.[11] Yet to move forward and possibly go beyond existing technologies will require the development of approaches that enable controlled assembly and integration of these building blocks on a scale far beyond that of individual or small numbers of devices produced by fluidic[12] and electric-field[13] directed assembly.

Here we report a solution-based approach for hierarchically organizing NW building blocks *en masse* into integrated arrays tiled over large areas. NWs were aligned with controlled nanometer to micrometer scale pitch using the Langmuir−Blodgett technique, transferred to planar substrates in a layer-by-layer process to form parallel and crossed NW structures over centimeter length scales, and then efficiently patterned into repeating arrays of controlled dimensions and pitch using photolithography. This solution-based method enables the specific NW building block, NW pitch, NW orientation, array size, array orientation, and array pitch to be controlled independently for sequential depositions, and thus offers a flexible pathway for bottom-up assembly of NW and nanotube materials into integrated and hierarchically organized structures.

Our approach for controlled assembly of NWs (Figure 1) exploits the Langmuir−Blodgett (LB) technique[14] to uniaxially compress a NW−surfactant monolayer on an aqueous subphase, thereby producing aligned NWs with controlled spacing. The compressed layer is then transferred in a single step to a planar substrate to yield parallel NWs covering the entire substrate surface. In addition, this sequence of steps can be repeated one or more times with controlled orientation to produce crossed and more complex NW structures, where the NWs can be the same or different in sequential layers. The ability to assemble a wide range of different NW building blocks in a flexible manner is a unique attribute of this bottom-up approach and quite distinct from top-down fabrication methods. The Langmuir−Blodgett technique was used previously to organize single layers of low aspect ratio nanorods into close-packed structures suggestive of liquid crystalline phases,[15] although this latter work did not demonstrate control of spacing and other properties critical to integrated and interconnected arrays. In addition, we have recently used this method to prepare large area NW masks for deposition and etching.[16]

We illustrate the flexibility of our approach using silicon NWs that were prepared with nearly monodisperse diameters by nanocluster catalyzed chemical vapor deposition.[17] Stable

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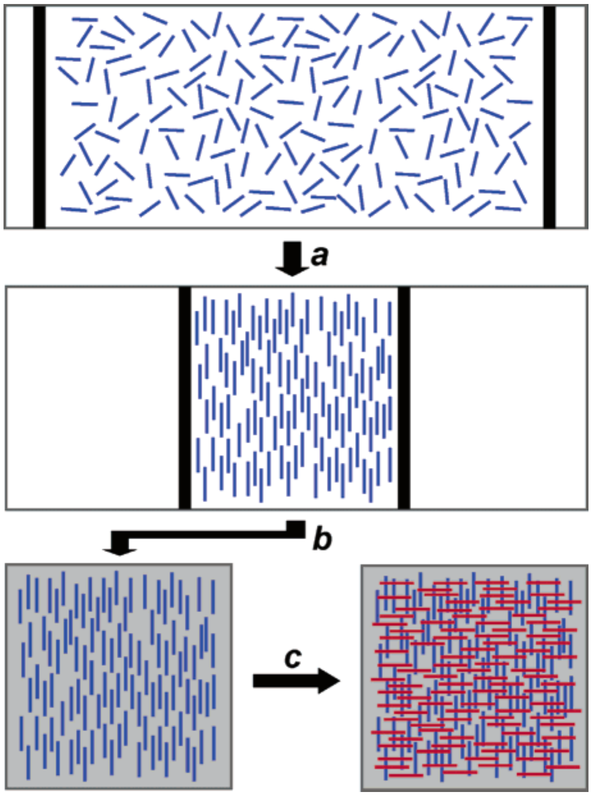

Figure 1. NWs (blue lines) in a monolayer of surfactant at the air–water interface are (a) compressed on a Langmuir–Blodgett trough to a specified pitch. (b) The aligned NWs are transferred to the surface of a substrate to make a uniform parallel array. (c) Crossed NW structures are formed by uniform transfer of a second layer of aligned parallel NWs (red lines) perpendicular to the first layer (blue lines).

NW suspensions in nonpolar solvents made using the surfactant 1-octadecylamine, which coordinates reversibly to NW surfaces, were spread on the surface of the aqueous phase in a Langmuir–Blodgett trough and compressed.[18] During compression, NWs become aligned along their long axes with the average spacing (center-to-center distance) controlled by the compression process. Large area field-emission scanning electron microscopy images (Figure 2A) show that parallel NWs were transferred with good uniformity and alignment onto substrates with areas up to 20 cm^2 in our experiments, although this approach can be applied to much larger area substrates.[19]

Significantly, we are also able to control the spacing of the transferred NWs from the micrometer scale to well-ordered and close-packed structures by the compression process. Representative images of transferred NWs with spacings of ca. 0.8 and 0.4 μm (Figures 2B, 2C) show that the NWs are isolated and have good uniaxial alignment. In general, we find that the transferred NW arrays have similar quality for spacings from ca. 2 μm (the largest studied) to 200 nm. Compression to spacings below ca. 200 nm leads to increasing aggregation due to strong inter-NW attractive forces, although aligned close-packed monolayer structures can be transferred. This latter capability was used to make ultrahigh-density arrays with the NW spacing controlled on the nanometer scale, by compressing NWs coated with

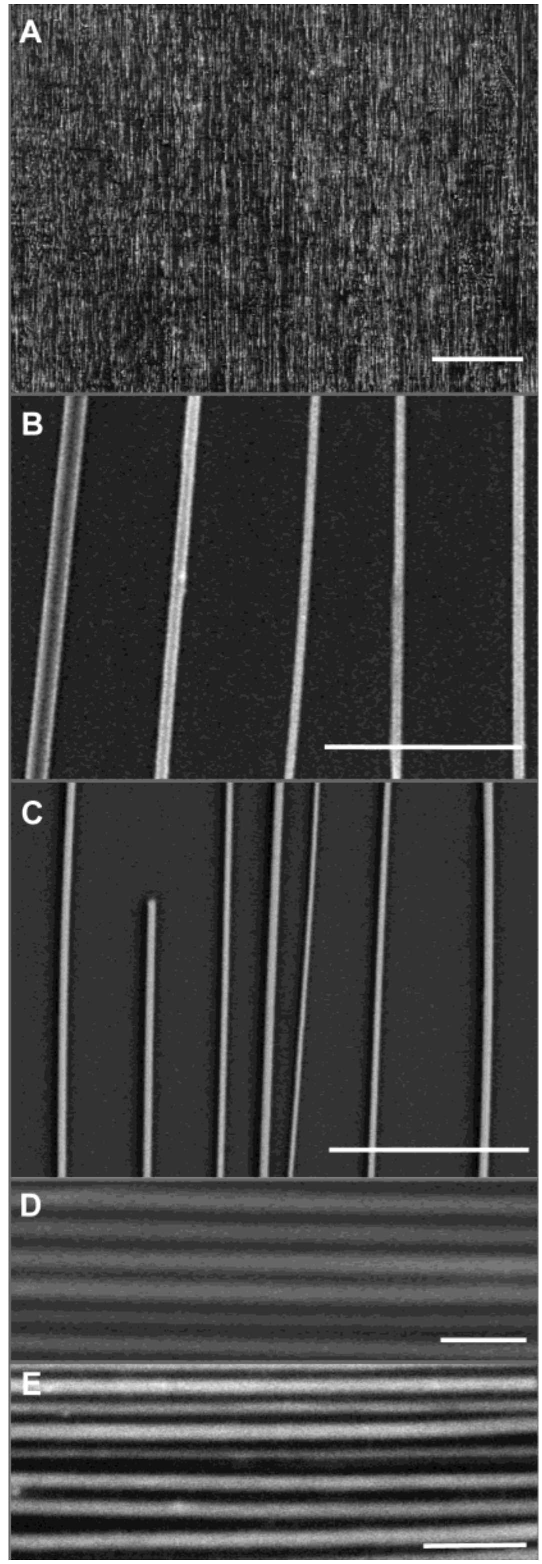

Figure 2. (A) Large area image of parallel NWs deposited uniformly on a 1 cm × 3 cm substrate. Scale bar, 100 μm. (B, C), Images of aligned parallel NWs transferred to substrates at different stages of LB compression. The scale bars in (B, C) correspond to 1 μm. (D, E) Images of high-density parallel NW arrays with average pitches of (D) ~90 and (E) ~45 nm; NWs with core diameters of 70 and 25 nm, respectively, and 10 nm silicon oxide shell thicknesses were used for assembly. The scale bars in (D, E) correspond to 200 nm. Images were recorded with a field-emission scanning electron microscope.

controlled thickness sacrificial layers, and then removing this layer once transferred.[16] For example, core/shell Si/SiO_2 NWs, in which the oxide shell thickness was precisely controlled during NW growth,[20] were compressed to close-packed structures and transferred to substrates. Images recorded following HF etching of the oxide shells show well aligned parallel NWs with center-to-center separations of 90 nm (Figure 2D) and ca. 45 nm (Figure 2E) that are in agreement with the values predicted based on the dimensions of the core/shell NWs; that is, the center-to-center separation is equal to 2 × (NW radius + shell thickness). We have also used selective dry (i.e., reactive ion) etching to remove oxide from core/shell Si/SiO_2 NWs to produce similar structures.[16] In addition, it should be possible to extend this approach to even finer spacings that would be difficult to achieve by top-down lithography.

The aligned, controlled spacing NW structures exhibit features similar to a nematic liquid crystal phase, including fluctuations in the average alignment direction and poor end-to-end registry (Figure 2C). These nonuniform features are distinct from the precise structures familiar to conventional top down fabrication; however, we do not believe these features represent serious impediments to making integrated and interconnected devices. Specifically, interconnected finite-size arrays of nanoscale devices are more desirable than monolithic structures for integrated nanosystems, because hierarchical organization reduces the probability that small numbers of defects will cause catastrophic failure in the whole system.[21] Hence, by adjusting this array size to be less than the average NW length it is possible to minimize the number of NWs that fail to span the width of an array due to poor end-to-end registry.

We have implemented this desired hierarchical patterning of the transferred NW structures in a flexible and scalable manner using photolithography (Figure 3). Following uniform transfer of NWs of a specified spacing onto a substrate, photolithography is used to define a pattern over the entire substrate surface, which sets the array dimensions and array pitch, and then the NWs outside the patterned array are removed by gentle sonication.[16,22] An image of a 10 μm × 10 μm square array with a 25 μm array pitch (Figure 3B) shows that this method provides ready and scalable access to ordered arrays over large areas. This array exhibits order on multiple length scales — 40 nm diameter NWs, 0.5 μm NW spacing, 10 μm array size, 25 μm array pitch repeated over centimeters — that is representative of the substantial control enabled by our approach. In addition, this approach can be used to define array geometries and tiling patterns more complex than the above square structures.

We have also investigated whether our new approach for assembling and patterning hierarchical NW arrays is compatible with fabrication of nanoelectronic devices. To test this important point, electron beam lithography was used to define a series of parallel finger electrodes contacting NWs in hierarchically patterned parallel arrays (Figure 3C). Electrical transport measurements carried out on three of the silicon NW devices exhibit linear current versus voltage behavior. This linear response and the typical two-terminal resistance

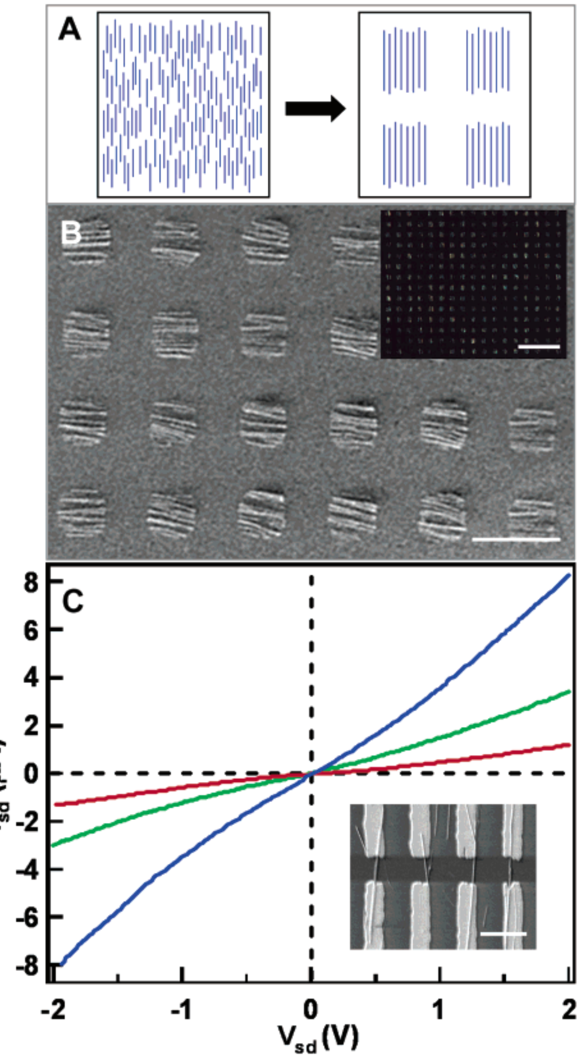

Figure 3. (A) Hierarchical patterning of parallel NW arrays by lithography, where NWs are removed from regions outside of the defined array pattern. (B) Image of patterned 10 μm × 10 μm parallel NW arrays. Scale bar, 25 μm. (inset) Large area dark-field optical micrograph of patterned parallel NW arrays. The inset scale bar is 100 μm. (C) Typical linear current vs voltage curves recorded from three NW devices. The resistance varies from 260 to 1780 kΩ for the blue, green, and red curves, respectively. Inset shows representative scanning electron microscopy image of four aligned NW devices defined by electron beam lithography; the scale bar is 3 μm.

values, 260−1780 kΩ, are indicative of good electrical contacts. We believe these preliminary results are important because they demonstrate that our solution-based hierarchical assembly methodology produces electrically active NWs, and therefore should be compatible with the goal of creating large-scale integrated, functional nanosystems. Significantly, recent studies using a scalable photolithography approach provide clear demonstration of this milestone.[23]

Last, our method can be used to make crossed NW arrays by transferring sequential layers of aligned NWs in an orthogonal orientation and then patterning the layers as described above (Figure 4A).[22] Crossed arrays are particularly attractive targets because previous small scale studies of crossed NW junctions have demonstrated interesting elec-

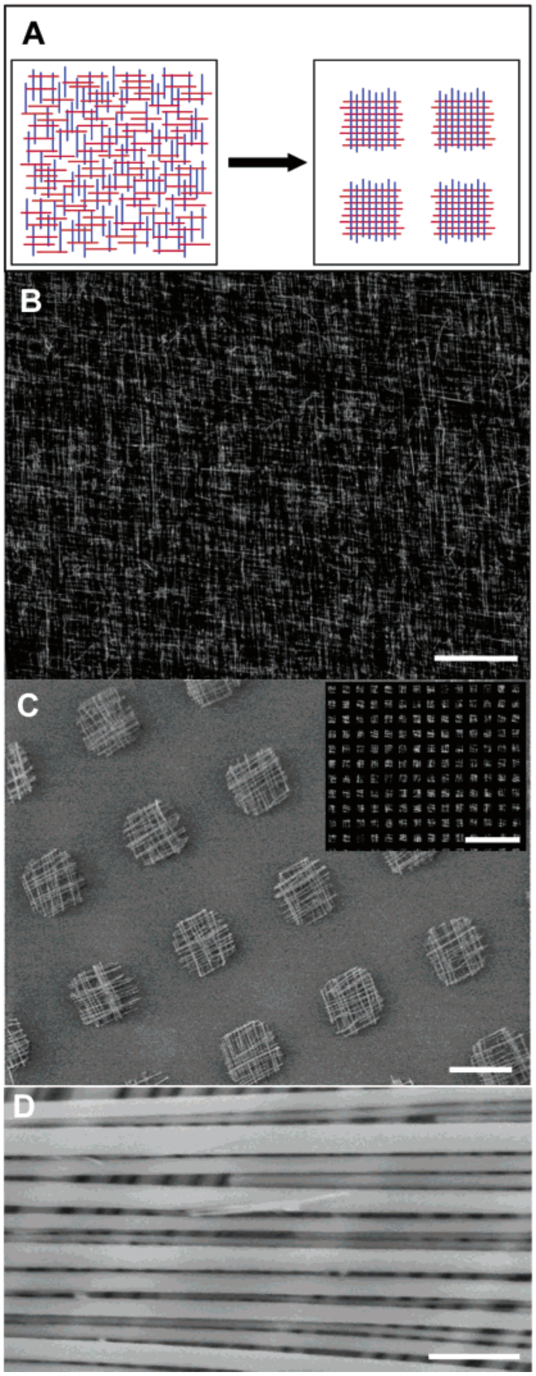

Figure 4. (A) Hierarchical patterning of crossed NW arrays by lithography, where NWs are removed from regions outside of the defined array pattern. (B) Dark-field optical micrograph of crossed NWs deposited uniformly on a 1 cm × 1 cm substrate; scale bar is 50 μm. (C) Scanning electron microscopy image of patterned crossed NW arrays; scale bar, 10 μm. (inset) Large area dark-field optical micrograph of the patterned crossed NW arrays; scale bar is 100 μm. (D) Scanning electron microscopy image of an ultrahigh-density crossed NW array; scale bar is 200 nm.

tronic[7] and photonic[6] function. Large area images of two silicon NW layers transferred sequentially with orthogonal alignment (Figure 4B) show that this approach yields relatively uniform coverage over centimeter length scales. Images of crossed NW arrays (Figure 4C), which were made by defining an array pattern with photolithography and then removing NWs outside of the patterned areas, show that regular 10 μm × 10 μm square arrays with a 25 μm array pitch can be achieved over large areas and that each of the square arrays consists of a large number of crossed NW junctions. In addition, we have made ultrahigh-density crossed NW arrays using the method described above. Close-packed Si/SiO_2 core/shell NWs were transferred in two orthogonal layers and then etched with HF to yield crossed NW arrays with pitches of less than 50 nm (Figure 4D). Because good electrical contacts to NW arrays assembled and patterned by our approach have been realized (Figure 3C), we believe it will be possible to create integrated nanosystems with diverse functions using these hierarchical crossed NW arrays in the future.

In summary, our studies have outlined a general and rational strategy for hierarchical organization of NWs and represent substantial progress toward the bottom-up assembly of integrated architectures over large areas in a highly parallel and scalable manner. The facile substitution of different NWs and changes in structural hierarchy enabled by this approach will be attractive for creating integrated, functional nanosystems. For example, crossed NW arrays could be used as addressable nanoscale light-emitting diode sources. More generally, efforts focused on increasing the structural complexity, for example by tiling functionally distinct arrays using additional transfer steps, could enable combinations of logic and memory arrays that are needed for nanocomputing[21] or even integrated sensing and processing function.

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Note Added after ASAP. Reference citations in the text have been corrected. This paper was originally posted ASAP on 8/5/03. The corrected version was posted on 8/14/03.

References

(1) McEuen, P. L. *Phys. World* **2000**, *13*, 31.
(2) Lieber, C. M. *Sci. Am.* **2001**, September, p 58.
(3) Avouris, Ph. *Acc. Chem. Res.* **2002**, *35*, 1026.
(4) Tans, S. J.; Verschueren, R. M.; Dekker, C. *Nature* **1998**, *393*, 49.
(5) Martel, R.; Schmidet, T.; Shea, H. R.; Hertel, T.; Avouris, Ph. *Appl. Phys. Lett.* **1998**, *73*, 2447.
(6) Duan, X.; Huang, Y.; Cui, Y.; Wang, J.; Lieber, C. M. *Nature* **2001**, *409*, 66.
(7) Cui, Y.; Lieber, C. M. *Science* **2001**, *291*, 851.
(8) Björk, M. T.; Ohlsson, B. J.; Thelander, C.; Persson, A. I.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. *Appl. Phys. Lett.* **2002**, *81*, 4458.
(9) Gudiksen, M. S.; Lauhon, L. J.; Wang, J.; Smith, D. C.; Lieber, C. M. *Nature* **2002**, *415*, 617.
(10) Hiruma, K.; Yazawa, M.; Katsuyama, T.; Ogawa, K.; Haraguchi, K.; Koguchi, M.; Kakibayashi, H. *J. Appl. Phys.* **1995**, *77*, 447.
(11) Duan, X.; Huang, Y.; Agarwal, R.; Lieber, C. M. *Nature* **2003**, *421*, 241.
(12) Huang, Y.; Duan, X.; Wei, Q.; Lieber, C. M. *Science* **2001**, *291*, 630.
(13) Smith, P. A.; Nordquist, C. D.; Jackson, T. N.; Mayer, T. S. *Appl. Phys. Lett.* **2000**, *77*, 1399.

(14) Ulman, A. *An introduction to ultrathin organic films: from Langmuir−Blodgett to self-assembly*; Academic Press: New York, 1991.
(15) Kim, F.; Kwan, S.; Akana, J.; Yang, P. *J. Am. Chem. Soc.* **2001**, *123*, 4360.
(16) Whang, D.; Jin, S.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 951.
(17) Cui, Y.; Lauhon, L. J.; Gudiksen, M. S.; Wang, J.; Lieber, C. M. *Appl. Phys. Lett.* **2001**, *78*, 2214.
(18) Single-crystal silicon NWs were synthesized by gold nanocluster catalyzed chemical vapor deposition with silane reactant.[17] Assembly was carried out using 20, 40, and 80 nm diameter NW samples. Stable solutions of the NWs were made from a 3:1 (v/v) mixture of isooctane and 2-propanol containing 1-octadecylamine (0.25 mM), which coordinates reversibly to the silicon NW surfaces. The solubility of the surfactant and resulting rate of the compression was controlled by the subphase pH. While the surface pressure was kept at constant value (55−60 mN/m), the area of the Langmuir monolayer was continuously reduced by the dissolution of the surfactant into the water subphase.
(19) Albrecht, O.; Matsuda, H.; Eguchi, K.; Nakagiri, T. *Thin Solid Films* **1996**, *284*, 152.
(20) Lauhon, L. J.; Gudiksen, M. S.; Wang, D.; Lieber, C. M. *Nature* **2002**, *420*, 57.
(21) DeHon, A. *IEEE Trans. Nanotech.* **2003**, *2*, 23.
(22) Shipley S1813 photoresist was deposited by spin coating (4000 rpm for 40 s) onto aligned NW covered substrates, baked at 110 °C for 4 min, and then exposed for ca. 2 s on an ABM photoaligner. After developing for 1 min, substrates were sonicated for 30 s in DI water to remove exposed NWs, and then the remaining photoresist covering the NW arrays was dissolved in acetone.
(23) Jin, S.; Whang, D.; Wu, Y.; McAlpine, M. C.; Friedman, R. S.; Lieber, C. M., submitted for publication.
(24) Silicon NWs used were grown[17] with diborane as the dopant source in a Si/B ratio of 2000:1. Electrode patterns were defined by electron beam lithography. Substrates were cleaned in an O_2 plasma (25 W for 60 s at 0.5 Torr O_2), etched in buffered HF (Transenes, Inc.) for 8 s, and then Ti/Au (50/30 nm) electrodes were deposited by electron beam evaporation.

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