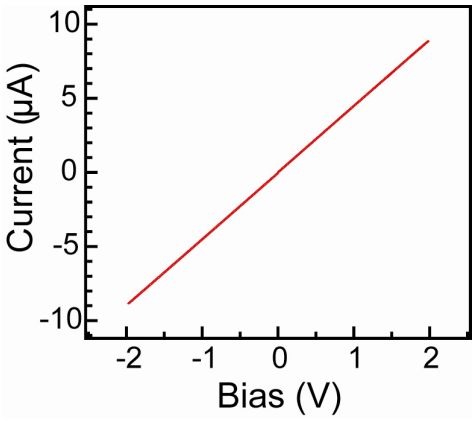

Figure S1. Current-voltage data recorded between two Ni contacts for a Si/a-Si NW. The linear behavior confirms that the Ni contacts to the NW are ohmic.

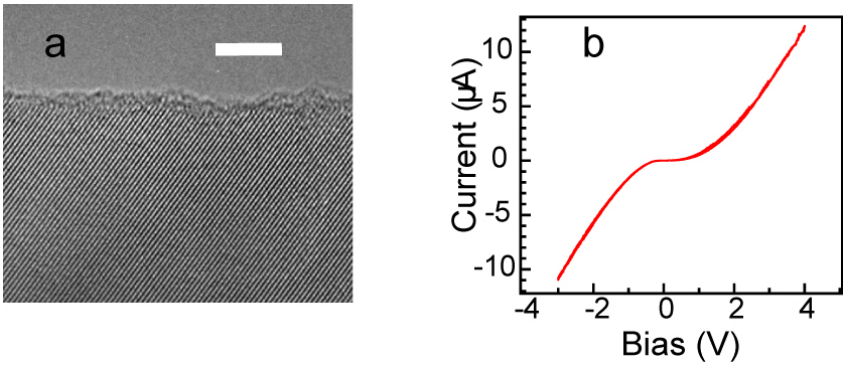

Figure S2. Si NW x M NW control devices. **a**, HRTEM image of a Si NW used in these experiments without the a-Si shell layer. Scale bar is 5 nm. **b**, Current-voltage data recorded between the ohmic (Ni) contact to the Si NW and the Ag NW electrode for a representative device. No switching was observed.

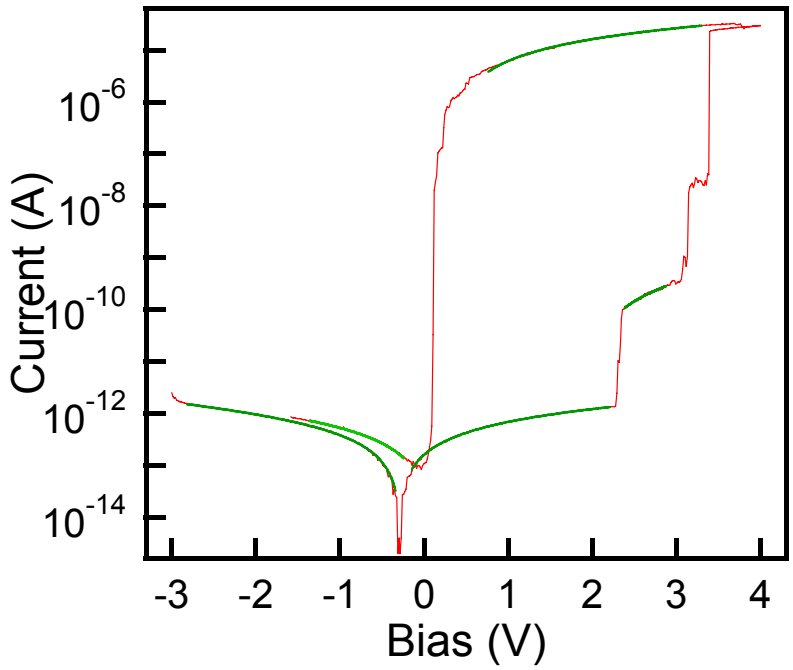

Figure S3. Analysis of the I-V data in Figure 2c. The raw data is shown in red and fits in green. A standard tunneling model[1] in which the current through the Si/a-Si x M junction is assumed to be limited by tunneling of electrons between the last metal island and the SiNW core electrode was used: $I = K \sinh k(V - V_0)$, where K and k are constants depending on the tunneling barrier height ϕ and the distance s between the last metal island and the SiNW core, and V_0 accounts for excess charges in the a-Si shell layer. The steps in the I-V data are consistent with the last metal island moving closer to the SiNW core.

1. Simmons, J. G.; Verderber, R. R. *Proc. R. Soc. London, Ser. A* **1967**, *301*, 77.

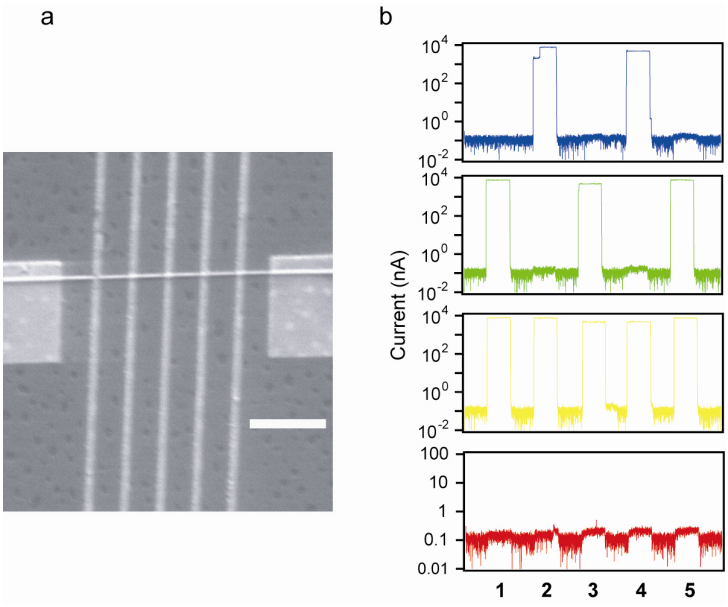

Figure S4. One dimensional memory array fabricated on a polyimide substrate (ref. 12, main text). **a**, SEM image of one Si/a-Si NW with five crossed metal lines. The image was taken after spin coating the plastic substrate with one layer of conductive polymer (ESPACER, Showa Denko). Scale bar is 2 μm. **b**, The states of the cross points 1-5 of the memory array are sequentially read out by a 2 V bias after writing or erasing them to arbitrary combination with a 4 or a -3 V pulse, respectively. (Blue: 01010, Green: 10101, Yellow: 11111, Red: 00000).