

# Si/a-Si Core/Shell Nanowires as Nonvolatile Crossbar Switches

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## ABSTRACT

Radial core/shell nanowires (NWs) represent an important class of nanoscale building blocks with substantial potential for exploring fundamental electronic properties and realizing novel device applications at the nanoscale. Here, we report the synthesis of crystalline silicon/amorphous silicon (Si/a-Si) core/shell NWs and studies of crossed Si/a-Si NW metal NW (Si/a-Si  $\times$  M) devices and arrays. Room-temperature electrical measurements on single Si/a-Si  $\times$  Ag NW devices exhibit bistable switching between high (off) and low (on) resistance states with well-defined switching threshold voltages, on/off ratios greater than  $10^4$ , and current rectification in the on state. Temperature-dependent switching experiments suggest that rectification can be attributed to barriers to electric field-driven metal diffusion. Systematic studies of Si/a-Si  $\times$  Ag NW devices show that (i) the bit size can be at least as small as  $20\text{ nm} \times 20\text{ nm}$ , (ii) the writing time is  $<100\text{ ns}$ , (iii) the retention time is  $>2\text{ weeks}$ , and (iv) devices can be switched  $>10^4$  times without degradation in performance. In addition, studies of dense one-dimensional and two-dimensional Si/a-Si  $\times$  Ag NW devices arrays fabricated on crystalline and plastic substrates show that elements within the arrays can be independently switched and read, and moreover that bends with radii of curvature as small as  $0.3\text{ cm}$  cause little change in device characteristics. The Si/a-Si  $\times$  Ag NW devices represent a highly scalable and promising nanodevice element for assembly and fabrication of dense nonvolatile memory and programmable nanoprocessors.

Semiconductor NWs and carbon nanotubes have been explored as building blocks that might extend the remarkably successful scaling of microelectronics industry and enable new paradigms for memory and processors.<sup>1–3</sup> An attractive architecture for exploiting the strengths of these one-dimensional (1D) building blocks for memory and logic consists of an array of crossed wires or crossbar.<sup>4–9</sup> In the context of memory, each cross point represents a bit where information can be stored and addressed. For example, a crossbar consisting of a set of parallel NWs or nanotubes on a substrate and a set of perpendicular carbon nanotubes that are suspended on a periodic array of supports can be electromechanically switched between stable on and off states.<sup>3c</sup> Structures in which molecular layers are sandwiched between crossed nanoscale wires also have been shown to exhibit hysteretic resistance switching,<sup>5</sup> where the mechanism of switching has been attributed to several effects, including charge-transfer-induced conformational change,<sup>6</sup> electro-mechanical switching,<sup>7</sup> and metal filament formation.<sup>8</sup>

The assembly of distinct NW elements into a crossbar represents a powerful alternative approach for memory and logic because key device features can be defined during the synthesis of NW building blocks and their subsequent assembly.<sup>3,9</sup> For example, the bit size in the crossbar structure is defined by the diameters of the orthogonal NWs and the electronic characteristics of the functional element are defined by the compositions of the two NWs (e.g., coaxial core/shell materials).<sup>2a</sup> Here, we illustrate this concept with the demonstration of cross point hysteretic resistance switches based on a core/shell NW–metal NW crossbar in which the core/shell NW core acts as one electrode contact, the shell, which can be controlled synthetically, functions as the storage medium, and the metal NW serves as the second electrode contact.

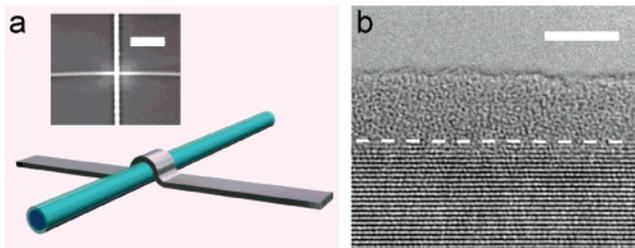
Our basic design shown in Figure 1a consists of a Si/a-Si core/shell NW and a lithographically defined crossed metal NW. The core/shell NWs used in this structure were synthesized in a two step chemical vapor deposition process developed previously,<sup>10</sup> which involves (i) metal nanocluster-catalyzed Si NW core growth followed by (ii) homogeneous deposition of the amorphous Si shell.<sup>11</sup> High-resolution transmission electron microscopy (HRTEM) imaging of the as-grown NW (Figure 1b) shows core/shell structure with

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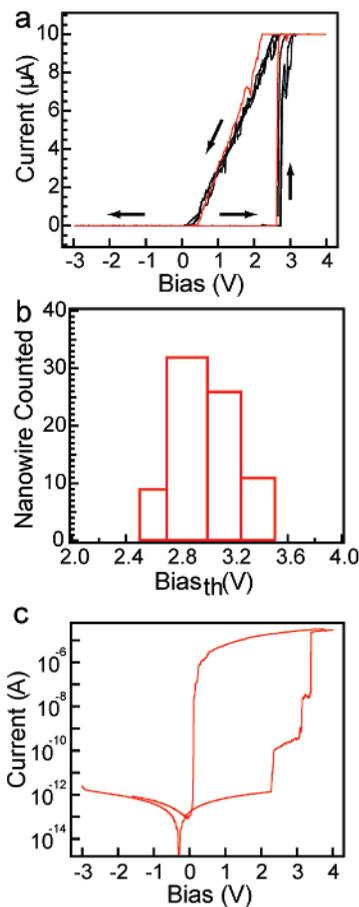


**Figure 1.** (a) A single switch is formed at the cross point of a Si (blue)/a-Si (cyan) core/shell NW and a metal NW (gray). (Inset) SEM image of a Si/a-Si NW (horizontal) crossed Ag-metal NW (vertical) device; scale bar is 1  $\mu\text{m}$ . (b) HRTEM image of a Si/a-Si core/shell NW. Dashed line indicates the interface between core and shell. Scale bar is 5 nm.

an  $\sim 5$  nm uniform amorphous silicon shell surrounding the single-crystal Si core and a sharp crystalline Si/a-Si interface. The Si/a-Si NWs were configured as cross point devices for electrical characterization in a hybrid bottom-up/top-down approach.<sup>12</sup> First, the core/shell NWs were assembled on a substrate using fluidic-based alignment<sup>9a</sup> and then Ni-metal contacts were defined at the NW ends; Ni was chosen as the contact metal because it readily forms ohmic junctions to Si NWs.<sup>13</sup> Second, an additional lithography step was used to define one or more crossed metal NWs.<sup>12</sup>

Representative current versus voltage ( $I$ - $V$ ) data obtained from a single Si/a-Si NW  $\times$  Ag NW device (Figure 2a) exhibits several key features. First, as the voltage is increased from 0 to 4 V, the current abruptly increases at  $\sim 3$  V. We define this abrupt transition point as the threshold voltage to switch the device from a high-resistance OFF state to a low-resistance ON state. Here voltage is defined as positive when the Ag NW is positively biased. Second, as the voltage is subsequently reduced to a negative threshold value ( $-3$  V in this case) the device switches back to the high-resistance OFF state. Third, the Si/a-Si NW  $\times$  Ag NW devices exhibit intrinsic current rectification; that is, the crossed NW devices show low conductance in the ON state when the applied voltage is negative (Figure 2a).<sup>14</sup> To the best of our knowledge, intrinsic rectification has not been observed previously for crossbar molecular structures,<sup>5c,15</sup> metal/a-Si/metal (M2M) or other metal/insulator/metal (MIM) devices.<sup>16</sup> Current rectification is an attractive property, because it can minimize cross talk between individual elements in arrays<sup>15</sup> and will be discussed further below. Fourth, switching between ON and OFF states is reproducible as exemplified by coincidence of initial cycle (red curve, Figure 2a) and three subsequent cycles (black curves, Figure 2a). The reproducibility of the switching in the Si/a-Si NW  $\times$  Ag NW structure was further confirmed by measurements on more than 80 devices. Notably, the histogram summarizing the threshold voltage (Figure 2b) exhibits a relatively tight distribution with a mean  $\pm 1$  standard deviation of  $3.0 \pm 0.5$  V and an overall yield of 95%.

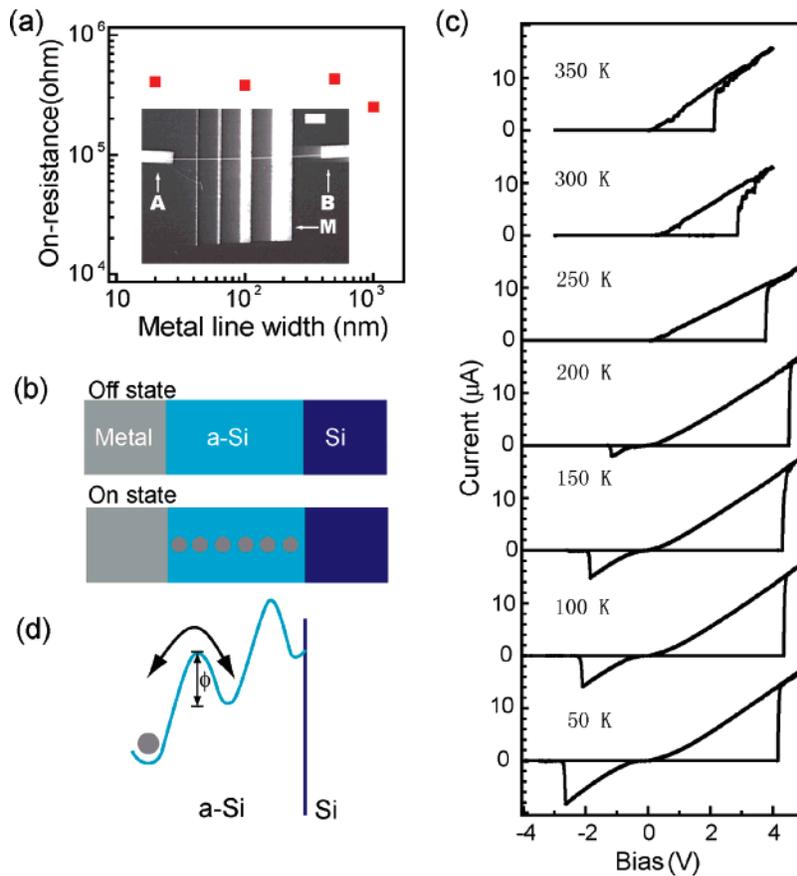
In addition, several other experiments were carried out to characterize basic crossed NW structure.  $I$ - $V$  data recorded between two Ni contacts show linear behavior (Supporting Information, Figure S1), which shows that there is no barrier between Ni and Si/a-Si core/shell NWs. Measurements made



**Figure 2.** (a) Current vs voltage sweeps where arrows indicate the voltage-scanning direction. The initial cycle is in red and subsequent three cycles are in black. (b) Histogram of the threshold voltage distribution from over 80 Si/a-Si NW  $\times$  Ag NW devices. (c) Current vs voltage cycle as in panel a but plotted on logarithmic scale.

on Si NW  $\times$  Ag NW structures (i.e., without the a-Si shell) show no switching or hysteresis (Supporting Information, Figure S2). These control experiments demonstrate that the observed switching can be attributed to the Si/a-Si NW  $\times$  Ag NW junction. Transport data recorded over a large dynamic range<sup>17</sup> and plotted on log scale (Figure 2c) highlight the large ON/OFF ratio, which can exceed  $10^6$  for a range of read voltages. Current rectification is also observed clearly in this data, which is consistent with Figure 2a; the rectification ratio obtained from the logarithmic data is  $> 10^6$  at  $\pm 1.5$  V. Finally, the transition from OFF to ON state exhibits several steps (Figure 2c) before the ON state is fully reached, which places a constraint on any mechanism used to describe switching within the Si/a-Si NW  $\times$  Ag NW junctions.

To probe further the Si/a-Si  $\times$  Ag NW structures, we investigated electrical transport characteristics as a function of the crossed junction size and temperature. First, current-voltage measurements made in a three-terminal geometry<sup>18</sup> demonstrate that the intrinsic junction resistance in the ON state is approximately independent of the junction size as the metal width is reduced from 1000 to 20 nm (Figure 3a). Constant junction resistance has been observed in previous



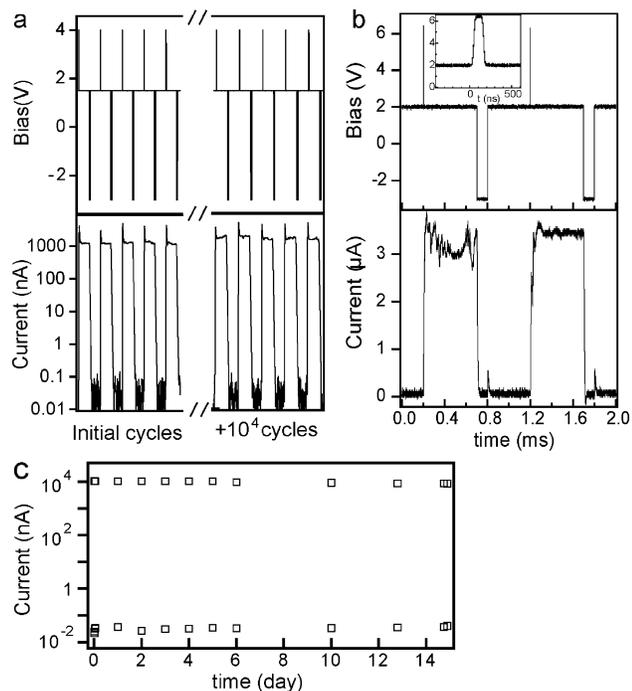
**Figure 3.** (a) ON state resistance for devices with metal NW widths of 20, 100, 500, and 1000 nm. The data were measured in a three-terminal configuration<sup>18</sup> to eliminate NW voltage drop. (Inset) SEM image of the device; scale bar is 1  $\mu\text{m}$ . A and B are ohmic contacts to the Si/a-Si NW, and M is the crossed metal NW. (b) Schematic illustrating the OFF and ON states for the Si/a-Si/metal junctions. The gray dots represent the silver islands that form the conducting filament in the ON state. (c)  $I$ - $V$  curves obtained on a single Si/a-Si  $\times$  Ag NW device as a function of temperature. (d) Schematic of barriers for the metal filament displacement in the a-Si adjacent to the SiNW core, where  $\phi$  corresponds to the barrier height and the arrow indicates direction of metal displacement.

studies of micron-scale M2M devices<sup>19</sup> and attributed to the formation of a metal filament, which defines the ON-state resistance. We believe that a similar mechanism (Figure 3b) is consistent with our data, although filaments in our case must be  $\leq 20$  nm (the smallest width Ag NW measured) in contrast to  $\sim 0.5$   $\mu\text{m}$  size observed in M2M devices.<sup>19</sup> A consequence of the proposed filament model shown in Figure 3b is that the current should be dominated by tunneling between the metal islands forming the filament (Figure 3b) as the device is driven to ON and then back to OFF states.<sup>16b</sup> The steplike changes in log-scale data (e.g., Figure 2c) as devices are turned on is consistent with the step-by-step filament formation as the metal is driven closer toward the core Si NW electrode.<sup>16,19</sup> Indeed, quantitative fits of the data in Figure 2c (Supporting Information, Figure S3) is consistent with this general model and tunneling dominated current as the device is stepwise turned ON and OFF.

Temperature-dependent current-voltage measurements were carried out to obtain further insight into the switching mechanism. Representative data acquired on a Si/a-Si  $\times$  Ag NW device (Figure 3c) show that the switching characteristics depend on temperature (Figure 2d). The turn-ON threshold voltage increased from  $\sim 3$  to  $\sim 4$  V as the temperature is reduced from 350 to 50 K. The increase in

turn-ON voltage is likely due to reduction of the Ag-ion diffusivity in the a-Si matrix, as reported previously in M/a-Si/M switching devices.<sup>20</sup> The magnitude of the current remains roughly constant from 350 to 50 K, consistent with the tunneling model. Of greater significance, as the temperature is reduced below 250 K the current rectification is lost and a more conventional resistor-like behavior is observed in the ON state. Qualitatively, these results can be explained within the context of the filament model as follows. Writing the device to the ON state at large positive biases results in the formation of a chain of metal islands that we assume are trapped in the a-Si matrix with an average energy barrier height  $\phi$  (Figure 3d). Because diffusion of the metal ions is a thermally activated process, it is possible for the metal ions to diffuse away from SiNW core at high temperatures and thereby yield a high-resistance state at small negative bias (the rectifying behavior). At sufficiently low temperatures, the filament is trapped in the ON state and does not exhibit rectification.

In addition, we have characterized key properties of the Si/a-Si  $\times$  Ag NW devices relevant to their potential use as nonvolatile switch/memory elements. First, the switching robustness was determined by repeating a cycle consisting of write, read, erase, and read steps as shown in Figure 4a,



**Figure 4.** (a) Write-read-erase-read cycles. The top curve shows the applied bias sequence for erase and write pulses, and the bottom curve shows corresponding current response read at 1.5 V. The measured OFF state current is limited by the dynamic range of the current amplifier used. (b) Writing speed test, where the upper curve shows sequence write and erase pulses, and the lower curve shows corresponding current response read at 2 V. (Inset) high-resolution measurement illustrating the temporal response of the write pulse. (c) Retention time test results for both ON and OFF states after writing or erasing the switch at +4 and  $-3$  V, respectively. Current is read at 2 V.

where the write, read, and erase voltages were +4, +1.5, and  $-3$  V, respectively. The current during the read step was  $10^{-6}$  A in the ON and  $<10^{-10}$  A in the OFF state. Notably, we find that the devices can be reliably switched between and read in ON and OFF states approximately  $10^4$  cycles without obvious degradation. Extending tests beyond  $10^4$  cycles typically results in increases in the OFF state current (and corresponding drop in the ON/OFF ratio). We believe that detailed studies of the changes in the a-Si layer associated with switching should provide insight into this degradation and may suggest changes that extend the number of cycles.

The device-switching speed was tested using a similar but fast write pulse in the write-read-erase-read sequence. As shown in Figure 3b, a 6.5 V write pulse of 100 ns can reproducibly turn on the device. Lower amplitude pulses, which are near the direct current switching threshold, were found to require a longer ca. microsecond duration to turn-on fully the devices. Further studies will be required to determine lower limit for the switching time. The retention time was also assessed in laboratory environment at room temperature. In these measurements, the device was disconnected from the power source after switching to ON or OFF states, and then the crossed NW resistance was periodically monitored. Notably, the data in Figure 4c demonstrate that the device had less than 20% decay in ON state after two

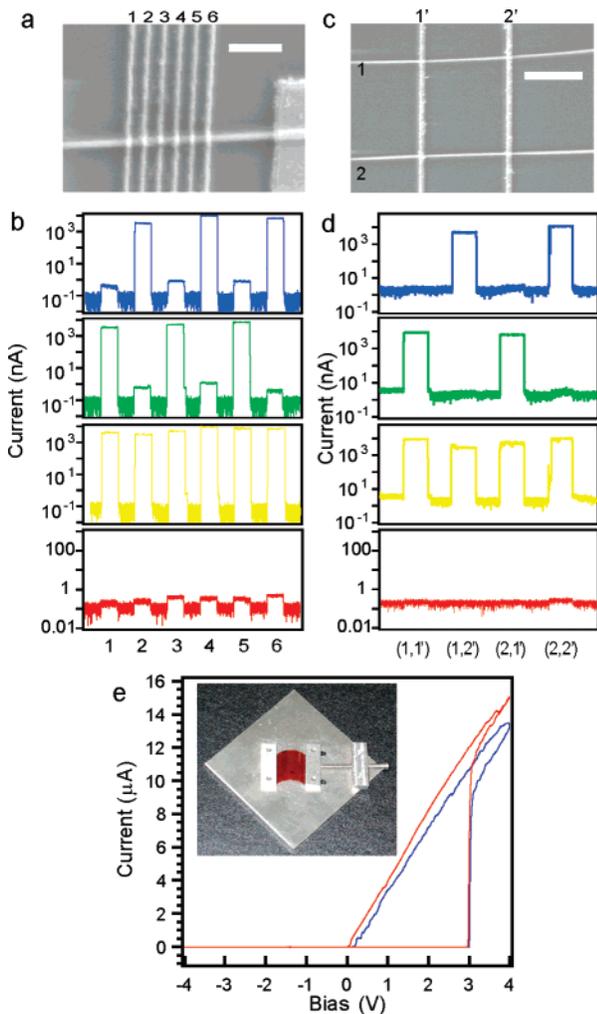
weeks and almost no change in OFF state thus confirming the nonvolatile nature of the Si/a-Si  $\times$  Ag NW devices.

The above results for our Si/a-Si  $\times$  Ag NW devices can be compared to molecular crossbar and M2M systems. Overall, the present endurance and retention times exceed those reported for molecular crossbar devices:  $10^4$  versus  $10-100$  and  $>2$  weeks versus several hours;<sup>5</sup> quantitative analysis of switching speeds have not been reported to the best of our knowledge. The observed NW device endurance and speed are comparable to those of optimally formed planar micron-scale M2M structures,<sup>16</sup> although our retention times are shorter. Furthermore, the crossed NW devices can survive scanning electron microscopy (SEM) inspection (electron energy 3 keV) for at least 30 min without obvious degradation, suggesting potential as radiation hard structures, similar to related M2M planar devices.<sup>21</sup>

The scalability of the Si/a-Si  $\times$  Ag NW device structure has been studied in 1D and 2D arrays. Relatively, dense 1D memory arrays were fabricated by crossing one Si/a-Si NW with  $n$  lithographically defined Ag NWs (denoted  $1 \times n$ ) such as Figure 5a, which shows a  $1 \times 6$  array with Ag NW width of 30 and 150 nm spacing. Transport measurements (Figure 5b) further show that it is possible to write or erase the six cross point switches to an arbitrary state (e.g., 000000, 111111, 101010, 010101 in Figure 5b) and then read the state of  $n$ -switches without cross talk between elements during writing, reading or erasing. A basic  $2 \times 2$  structure (Figure 5c) was also fabricated to investigate whether the intrinsic rectification exhibited by Si/a-Si  $\times$  Ag NW elements can eliminate cross talk in a 2D array. Notably, Figure 5d shows that starting from the OFF state (0000), an arbitrary combination (e.g., 1111, 1010, 0101) of bits can be written into the array and then read out. While the density of this test array is low, recently demonstrated directed-assembly methods<sup>22</sup> suggest that it should be possible to prepare much denser 2D arrays and even to extend the results to 3D layer-by-layer structures.

Last, we note that our approach to SiNW-based crossbar switches is not limited to conventional crystalline substrate because the high-temperature NW synthesis is separate from the low-temperature fabrication process.<sup>23</sup> To this end we have assembled Si/a-Si  $\times$  Ag NW devices on flexible plastics and characterized their device properties. One-dimensional arrays fabricated on Kapton polyimide substrates (Supporting Information, Figure S3) showed that it is possible to write, read, and/or erase each of the five bits without cross talk. Moreover, comparison of the switching cycles recorded when the device substrate was flat versus bent to a radius of curvature of 0.3 cm (Figure 4e) shows little change in the threshold voltage and only a slight decrease ( $\sim 10\%$ ) in ON state current for the device in the bent configuration. These latter results demonstrate clearly the potential of these devices for development of flexible nonvolatile memory.

In summary, we have reported the synthesis of crystalline silicon/amorphous silicon (Si/a-Si) core/shell NWs and studies of crossed Si/a-Si NW metal NW (Si/a-Si  $\times$  M) devices and arrays. Room-temperature electrical measurements on single Si/a-Si  $\times$  Ag NW devices demonstrated



**Figure 5.** (a) SEM image of a  $1 \times 6$  array composed of one Si/a-Si NW crossing six Ag NWs. Scale bar is 500 nm. (b) States of cross points 1–6 read at 2 V: blue = 010101, green = 101010, yellow = 111111, and red = 000000. (c) SEM image of two Si/a-Si NWs (horizontal) and two Ag NWs (vertical) in a  $2 \times 2$  array. Scale bar is  $1 \mu\text{m}$ . (d) State of the four cross points read at 2 V: blue = 0101, green = 1010, yellow = 1111, and red = 0000. (e)  $I$ – $V$  curves for a Si/a-Si  $\times$  Ag NW device measured when the substrate was flat (red) and bent to a 0.3 cm radius of curvature (blue). (Inset) Photograph of a bent  $1.2 \text{ cm} \times 1.5 \text{ cm}$  flexible plastic substrate prior to measurement.

bistable switching between high (OFF) and low (ON) resistance states with well-defined switching threshold voltages, ON/OFF ratios greater than  $10^4$ , and current rectification in the ON state. Systematic studies of Si/a-Si  $\times$  Ag NW devices show that (i) the bit size can be at least as small as  $20 \text{ nm} \times 20 \text{ nm}$ , (ii) the writing time is  $< 100 \text{ ns}$ , (iii) the retention time is  $> 2$  weeks, and (iv) devices can be switched  $> 10^4$  times without degradation in performance. In addition, studies of dense 1D and 2D Si/a-Si  $\times$  Ag NW device arrays fabricated on crystalline and plastic substrates show that elements within the arrays can be independently switched and read, and moreover that bends up with radii of curvature as small as 0.3 cm cause little change in device characteristics. The Si/a-Si  $\times$  Ag NW element represents a highly scalable and promising nanodevice with potential for dense nonvolatile memory and programmable nanoprocessors.

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**Supporting Information Available:** Electrical characterization of Ni device contacts (Figure S1). Control experiment results using NWs without a-Si layer (Figure S2). Analysis of the  $I$ – $V$  data in Figure 2c with the tunneling model (Figure S3). One-dimensional array fabricated on flexible plastic substrate (Figure S4). This material is available free of charge via the Internet at <http://pubs.acs.org>.

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- (11) Si/a-Si core-shell NWs were grown using methods similar to other core-shell heterostructure NW growth.<sup>10</sup> The Si core was grown at  $435 \text{ }^\circ\text{C}$  for 20 min using silane (2 sccm) and 100 ppm of diborane in helium (10 sccm) at 20 torr, yielding an axial growth rate of about  $1 \mu\text{m}$  per minute. The a-Si shell was grown at  $450 \text{ }^\circ\text{C}$  for 5 min at 15 torr using the same reactant flow rate. The growth rate of the a-Si shell is about 1 nm per minute. Growth of NWs used for control experiments omitted the shell growth step. The as-grown NWs were dispersed in ethanol by sonication. HRTEM characterization (JEOL 2010F) was performed with the NWs deposited on copper grids.
- (12) The device fabrication was carried out by two-step electron beam (e-beam) lithography (Raith 150 Ebeam) after the NWs were deposited on oxidized silicon or  $125 \mu\text{m}$  polyimide (500-FPC, Kapton) substrates. The first lithography step defined the electrical contacts to the NWs, followed by wet etching (buffered HF, 15 s), and thermal evaporation of Ni (60 nm thick). The devices were subsequently annealed at  $350 \text{ }^\circ\text{C}$  for 60 seconds in forming gas ( $\text{N}_2/\text{H}_2$ , 90/10%), (Heatpulse 610, Metron Technology) to facilitate better ohmic contacts to the Si core. Ag (60 nm) NWs were then defined

in the second e-beam lithography step and deposited above the a-Si shell without etching and annealing. For the  $2 \times 2$  array fabrication, the NWs were first flow-aligned.<sup>9a</sup> SEM imaging or e-beam writing on Kapton substrates used a layer of conductive polymer (ESPACER, Showa Denko) to avoid charging.

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- (17) Measurement of the basic  $I$ - $V$  curves, endurance cycles, and retention times test of the device were carried out in air with a probe station (TTP-4, Desert Cryogenics, Tucson, AZ), using either a home-built measurement setup with a current amplifier (DL instruments 1211, Ithaca, NY) or a high-precision semiconductor analyzer (Agilent 4156C, Agilent Technologies, Palo Alto, CA). Temperature-dependence measurements were carried out under vacuum ( $<1 \times 10^{-4}$  torr). The nanosecond voltage pulses were generated with an Agilent 33220A function generator and the current signal recorded on a Tektronix TDS 3012 oscilloscope.
- (18) In the three terminal measurements, the current  $I$  flows between the metal line (M) and the right ohmic contact (B), and the voltage  $V_{M-A}$  is measured between M and the left ohmic contact (A), such that  $V_{M-A}$  reflects the actual voltage drop at the Si/a-Si  $\times$  M junction and not contributions from the NW series resistance. The on-resistance  $R_{on}$  was measured as  $V_{M-A}/I$  at  $V_{M-A} = 2$  V in the on-state.
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