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Review Paper

Large-Scale Hierarchical Organization of Nanowires for Functional Nanosystems

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We review recent studies of solution-based hierarchical organization of nanowire building blocks. Nanowires have been aligned with controlled nanometer to micrometer scale separation using the Langmuir-Blodgett technique, transferred to planar substrates in a layer-by-layer process to form parallel and crossed nanowire structures over centimeter length scales, and then efficiently patterned into repeating arrays of controlled dimensions and pitch using photolithography. The hierarchically-organized nanowires open up key opportunities in several general areas of nanoscale science and technology. First, hierarchically-assembled nanowire arrays have been used as masks to define nanometer scale metal lines and surface features over large areas. Second, hierarchically-assembled nanowire arrays have been used to fabricate fully-scalable centimeter size arrays of field-effect transistors in high yields without requiring alignment of individual nanowires to output electrodes. Diverse applications of this approach for enabling a broad range of functional nanosystems, including macroelectronic and sensing applications, are described. [DOI: 10.1143/JJAP.43.4465]

KEYWORDS: assembly, Langmuir-Blodgett, building blocks, nanowires, nanolithography, hierarchical arrays, large-scale integration

1. Introduction

Microelectronics today has been driven by innovations in "top-down" manufacturing processes. In order to increase the density of functional devices, improve the processing power, and reduce the cost of manufacturing, the features lithographically patterned on bulk semiconductor materials have been shrunk by more than two orders of magnitude over the last several decades.[1)] However, this remarkable trend of miniaturization may soon come to the end due to fundamental physical and/or economic limitations.[1–3)] Alternatively, "bottom-up" approaches,[3–6)] in which integrated functional device structures are assembled from chemically synthesized nanoscale building blocks, such as carbon nanotubes (NTs)[7–12)] and semiconductor nanowires (NWs),[13–22)] have the potential to revolutionize the fabrication of electronic and photonic systems and to enable a wide range of technological applications. It is in this context of bottom-up paradigm for nanoscience and nanotechnology that we will discuss general schemes for the hierarchical organization of one-dimensional nanoscale building blocks for functional nanosystems.

NWs and NTs have been extensively studied as building blocks for a number of nanoscale devices.[4,7–22)] Semiconductor NWs are especially attractive building blocks since these materials can be synthesized in single-crystalline form with precisely controlled structures, diameters and lengths, chemical compositions and doping/electronic properties using a nanocluster catalyzed vapor-liquid-solid growth process.[4)] This control over the growth of NWs has enabled the bottom-up assembly of integrated electronic and photonic devices, including nanometer scale field-effect transistors (FETs),[13,14)] *p-n* diodes,[14,15)] bipolar junction transistors,[15)] bistable switching devices,[16)] integrated logic circuits,[16,17)] address decorders,[18)] light-emitting diodes,[14,19)] electrically driven lasers,[20)] sensors.[21,22)] However, most studies of NWs and NTs have been limited to the demonstration of single or small numbers of nanodevices using serial lithographic processing, such as electron-beam lithography, to contact random structures on a substrate. To provide directional control over NW and NT building blocks during assembly several groups have used electric-fields[14,23,24)] and fluid flows within microfluidic channels.[25)] However, these methods have only led to relatively small scale structures without hierarchical control, and thus do not address many of the critical needs required for the assembly of integrated nanosystems.[4–6)]

Here we review recent progress[26–28)] from the authors' laboratory focused on the development of a general and efficient solution-based approach for hierarchically organizing NW building blocks *en masse* and integration of the resulting structures into functional device arrays over large areas.

2. Assembly of Nanowires Using the Langmuir-Blodgett Method

In order to go beyond the limited successes achieved previously in the assembly of NWs and NTs,[14,23–25)] we have utilized the well-established Langmuir-Blodgett (LB) technique for the assembly of nanoscale building blocks. The LB approach[29)] is attractive since (i) ordered monolayers can be formed over large area, (ii) the organized monolayers can be easily transferred to substrates, and (iii) the ordering and transfer processes can be repeated to yield multiple layers of the same or distinct materials.

The underlying concept of our approach for assembly of NWs using the LB method is illustrated in Fig. 1.[26)] Stable nonpolar NW suspensions, which are achieved using surfactants, are dispersed onto an aqueous subphase in a LB trough and the NW-surfactant monolayer formed on the air/water interface is then uniaxially compressed. During the compression, directional shear flow of the Langmuir monolayer is induced and yields NWs aligned perpendicular to the compression direction. In addition, the average spacing between NWs can be also controlled by reducing the area of the Langmuir monolayer, for example, by slow dissolution of the surfactant into the water subphase. The layer of aligned NWs is then transferred in a single step to a planar substrate to yield parallel NWs covering the entire substrate surface. Notably, this sequence of steps can be repeated one

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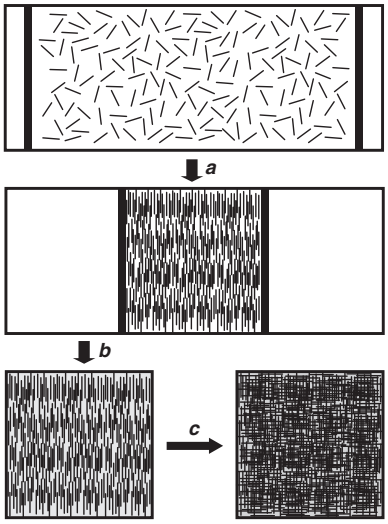

Fig. 1. Assembly of NWs. NWs (lines) at the air-water interface are (a) uniaxially-compressed to a specific pitch. (b) The aligned NWs are transferred to a substrate surface to form a uniform parallel array. (c) Crossed NW structures are formed by transfer of a second layer of aligned NWs perpendicular to the first layer.

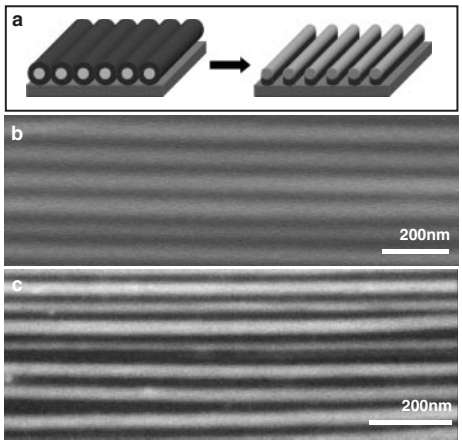

Fig. 3. High-density parallel NW arrays. (a) Schematic illustrating a close-packed NW array on a substrate, where the NWs consist of a functional core (gray) and sacrificial shell (black), and subsequent removal of the shell to yield ultrahigh density NW array. (b, c) SEM images of high-density parallel NW arrays with average pitches of (c) ~90 and (d) ~45 nm.

or more times with controlled orientation using virtually any NW building block to produce crossed and more complex NW arrays with functions determined by the NWs chosen for the different assembly steps.

We have demonstrated this approach using silicon NWs.[30] Scanning electron microscopy (SEM) images show that aligned NWs were transferred uniformly onto large substrates in our experiments (Fig. 2(a)), and the spacings of the transferred NW arrays were also controlled from the micrometer to nanometer scale by the compression process (Figs. 2(b) and 2(c)). Our method can be readily extended in a scalable manner to ultra-dense NW arrays with controlled regular spacing. Our approach for achieving this control on the nanometer scale involves coating NWs with sacrificial layer of controlled thickness prior to LB assembly, compression of the nanowires to an aligned close-packed structure, transfer to a substrate, and then removal of the sacrificial layer (Fig. 3(a)). Well-aligned parallel NWs with controlled pitches of smaller than 100 nm (Figs. 3(b) and 3(c)) were made following deposition of close-packed Si/SiO_2 core/shell NWs,[31] in which the SiO_2 shell thickness was precisely controlled, and subsequent etching to remove the oxide, though the arrays could be scaled to even higher densities using smaller diameter NWs.

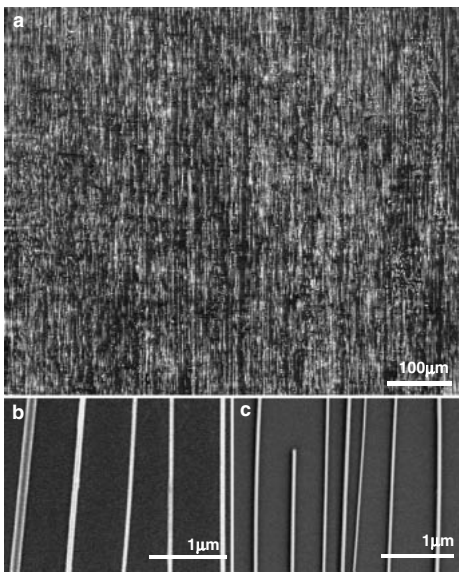

Fig. 2. Deposition of controlled separation parallel NWs. (a) Large area SEM image of parallel NWs deposited uniformly on a substrate. (b, c) Images of aligned parallel NWs transferred to substrates at different stages of LB compression, with average separation of ca. (b) 0.8 and (c) 0.4 μm.

3. Assembled Nanowires as Masks for Nanolithography

The development of novel methods for patterning structures on nanometer length scales can make possible fundamental investigations of new devices and could help to enable applications in nanoelectronics, photonics and nano-biotechnology. It is possible to pattern nanometer scale features using the NW arrays as masks for deposition and etching.[27] Following transfer of uniaxially-aligned NWs with controlled separation to a substrate, the NWs can be used as masks to transfer the line-pattern to the underlying substrate surface by etching, or alternatively, other materials, such as metals, can be deposited using the aligned NWs as shadow masks to create arrays of nanoscale wires. The NW masks are removed by isotropic wet etching and sonication to expose the etched or deposited parallel line features at the end of these steps. A clear illustration of the flexibility of this approach is illustrated in Fig. 4, where assembled NWs were used to define the deposition of parallel metal lines with average widths and pitches as small as 40 and 90 nm, respectively. Thin metal films were deposited using the aligned NWs as shadow masks to create arrays of nanoscale wires.

These studies demonstrated several important characteristics of our NW-based lithography approach using large-scale assembled NWs. First, the line width and pitch can be well-controlled via the synthesis of NWs and subsequent

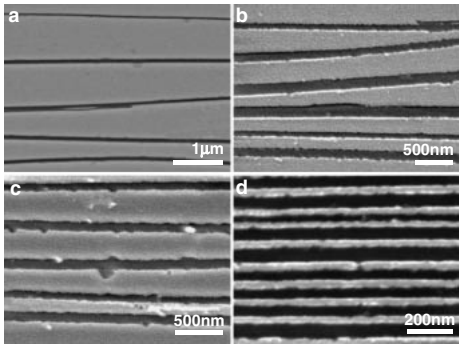

Fig. 4. SEM images of Cr-metal stripes with pitches of (a) ~600, (b) 300, (c) 200, and (d) 90 nm. Brighter areas in the images correspond to the 15 nm thick Cr-metal lines.

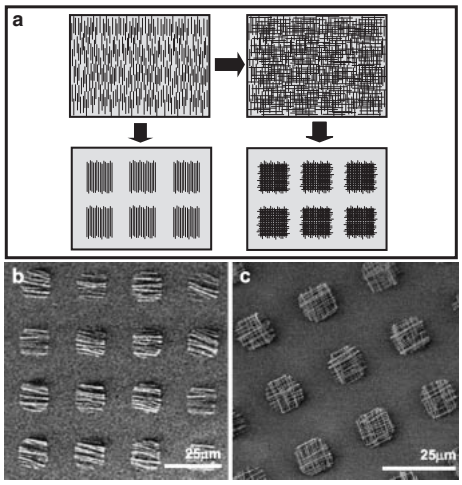

Fig. 5. (a) Hierarchical patterning of parallel and crossed NW arrays. (b) SEM image of patterned 10 μm × 10 μm parallel NW arrays. (c) SEM image of patterned 10 μm × 10 μm crossed NW arrays.

assembly steps. This offers the potential for rapidly and independently changing the line width and pitch down to the nanometer scale. Second, the smallest feature sizes defined by our method are comparable to state-of-art extreme UV lithography and approach the limit of electron-beam lithography. Third, LB approach can be used to assemble NWs in one-step over areas of at least 20 cm^2, which exceeds most other unconventional lithography methods. Hence, this nanolithography method represents a highly scalable and flexible approach for defining nanometer scale lines on multiple lengths scales and thus has substantial potential for enabling the fabrication of many types of periodic nanostructures and integrated nanosystems.

4. Hierarchical Patterning of Nanowire Arrays

The aligned, controlled spacing NW structures produced by LB assembly method exhibit features similar to a nematic liquid crystal phase, including fluctuations in the average alignment direction and poor end-to-end registry (Fig. 2(c)). These non-uniform features are distinct from the precise structures familiar to conventional top-down fabrication; however, these features do not represent serious impediments to making integrated and interconnected devices. Specifically, interconnected finite-size arrays of nanoscale devices are more desirable than monolithic structures for integrated nanosystems, because hierarchical organization reduces the probability that small numbers of defects will cause catastrophic failure in the whole system. Hence, by adjusting the array size to be less than the average NW length it is possible to minimize the number of NWs that fail to span the width of an array due to poor end-to-end registry.

We have implemented this desired hierarchical patterning of the transferred NW structures using photolithography (Fig. 5(a)). Following uniform transfer of NWs of a specified spacing onto a substrate, photolithography is used to define a pattern over the entire substrate surface, which sets the array dimensions and array pitch, and then the NWs outside the patterned array are removed by gentle sonication. An image of a 10 μm × 10 μm square array with a 25 μm array pitch (Fig. 5(b)) shows that this method provides ready and scalable access to ordered arrays over large areas. This array exhibits order on multiple length scales — 40 nm diameter NWs, 0.5 μm NW spacing, 10 μm array size, 25 μm array pitch repeated over centimeters — that is representative of the substantial control enabled by our approach. In addition, this approach can be used to define array geometries and tiling patterns more complex than the above square structures.

Our method can also be used to deposit sequential layers of aligned NWs in which the specific nanowire properties and array orientation are varied. This capability, which is advantageous over transfer lithography approaches, could enable large crossed NW arrays needed for implementing electronic and photonic nanosystems based upon previously reported crossed NW junctions.[15,17,18] To this end we have carried out assembly and hierarchical patterning of crossed NW arrays using the layer-by-layer scheme illustrated in Fig. 5(a). First, aligned, parallel NWs were transferred in sequential orthogonal directions onto a substrate surface. Second, crossed NW arrays and tiling patterns were defined using photolithography, and NWs outside the pattern were removed to produce regular square arrays over large areas, in which each square array consists of a large number of crossed NW junctions (Fig. 5(c)). In this general process, the different levels of hierarchy and patterning can be readily changed and different NW building blocks can be substituted in a facile manner, both of which are essential for the general assembly of integrated and functional nanosystems.[4,5]

5. Large-Scale Integration of Nanowire Devices without Registration

Device integration approaches that are fully scalable in terms of device density and area of coverage are essential for the development of functional nanosystems assembled from the bottom-up.[3–6] Previously reported studies of NW and NT FETs have used serial electron beam lithography to define interconnects, and have thus precluded studies of large systems.[8–10,12–14] To overcome this substantial issue, we developed a new strategy that has enabled parallel and scalable integration of NW devices over large areas without the need to register individual nanowire-electrode interconnects.[28] This approach exploits the Langmuir-Blodgett method described above to organize NWs with controlled alignment and spacing over large areas, and parallel photolithography to define interconnects in a statistical manner.

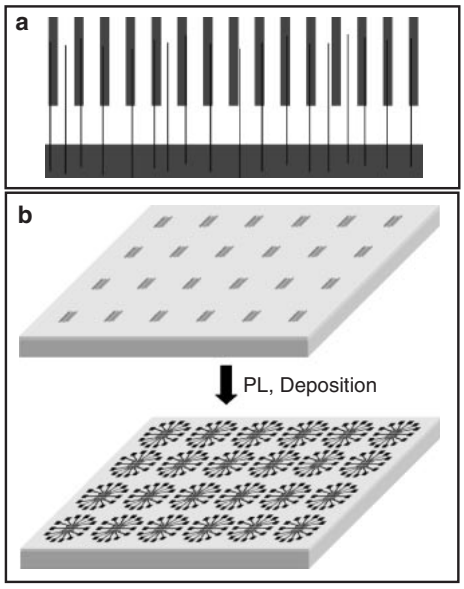

Fig. 6. Parallel and scalable interconnection of NW devices without registration. (a) Central electrode region of a single array emphasizing the high fraction of interconnected NWs obtained without the registration of individual electrodes. (b) Schemetic illustrating a key step of the deposition of repeating metal electrode array defined using photolithography (PL).

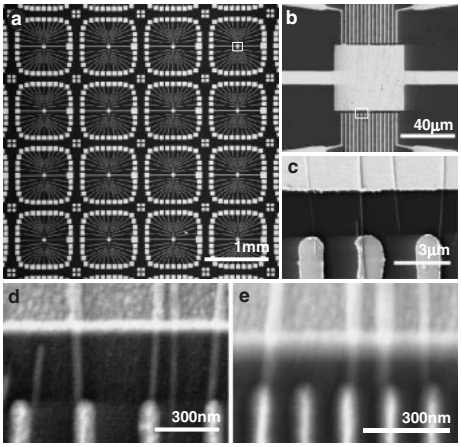

Fig. 7. (a) Optical micrograph of integrated metal electrode arrays deposited on top of patterned parallel NW arrays defined by photolithography. (b) SEM image of the central active region of a repeat unit of the electrode array show in part a. (c) Image of three NW devices connected between the common and finger electrodes. (d, e) Images of higher-density NW devices defined by electron been lithography.

Our approach to large-scale and parallel interconnection exploits the fact that the separation between NWs assembled by the Langmuir-Blodgett method has a defined average value but varies on the local scale. In this context, it is possible to achieve a high yield of metal electrode-to-nanowire contacts simply by setting the average NW separation to a value comparable to the electrode width (Fig. 6(a)); that is, the local fluctuations in separation lead to an efficient formation of contacts. There are two key features in this approach. First, it is not necessary to register the metal electrodes, which are defined by conventional lithography, to individual NWs in an array to achieve a high yield of contacts; only the position of the electrodes relative to a group of aligned NWs needs to be fixed. Second, the approach is intrinsically scalable to large areas since each of the key steps (Fig. 6(b)) can be carried out over an entire substrate or wafer in parallel.

This approach has been demonstrated with the fabrication of large arrays of NW FETs in which each active device consists of a single p-type silicon NW.[28] Optical and electron microscopy images (Figs. 7(a)–7(c)) demonstrate the key features and hierarchy of structures produced by our approach, including (1) FET sub-arrays with a 1 mm array pitch repeated over the entire substrate, (2) central electrode arrays on a 3 μm electrode pitch, and (3) individual 20 nm diameter NWs connected between the finger electrodes. Figure 7(c) illustrates that single NWs can fall between two metal electrodes as expected statistically, although the overall NW alignment prevents such 'defective devices' from adversely affecting properly interconnected NWs. Using this method, approximately 80% of the 3000 possible electrode connections available on a typical test chip could be bridged by NWs when the spacing of the aligned NWs was closely matched to the electrode width.

Our basic approach is scalable and thus can be used to produce devices in the nanometer size regime over large areas. Since the average NW spacing can be controlled down to the nanometer scale during the Langmuir-Blodgett compression, much smaller device size and higher density of device integration can be readily achieved when existing high resolution parallel lithography techniques, such as submicron photolithography, extreme-UV lithography[32] or nanoimprint lithography,[33] are applied to define electrodes following this interconnection strategy. To demonstrate this key point of scaling, we used electron beam lithography to define regular nanometer scale contact electrodes without registering to individual NWs to produce individual NW devices with a 300 nm (Fig. 7(d)) and 150 nm (Fig. 7(e)) pitch in high-yield.

High performance devices were achieved in high yields for the massive arrays of FETs fabricated via this approach. Electrical characterization of randomly chosen NW devices within the large arrays (Fig. 8) show expected[34] current-voltage characteristics for high performance p-type field-effect transistors that rival state-of-the-art planar silicon devices:[35] on/off current ratios greater than 10^6 and substhreshold slopes of below 250 mV/decade. A histogram of the observed peak transconductance values (Fig. 8(b) inset) shows a most probable value close to 1000 nA/V and a maximum value of 4300 nA/V corresponding to a calculated hole mobility of 307 $cm^2/V{\cdot}s$.

We have also fabricated pixel-like arrays (Fig. 9(a)), in which interdigitated electrodes were used as contacts to the patterned NWs so that the number of NW devices per 'pixel transistor' can be readily varied by controlling the NW spacing prior to deposition of the contact electrodes. Since the NW devices behave reproducibly, it is possible to scale key device characteristics, such as the transistor on-current, in this way. Transfer of aligned NWs with a relatively large (Fig. 9(b)) and small (Fig. 9(c)) average NW spacings yielded devices with a few NWs and 30–40 NWs, respectively, bridging each set of interdigitated electrodes. The significant differences in on-currents (6 μA vs 37 μA) demonstrate excellent scaling of properties in the multi-

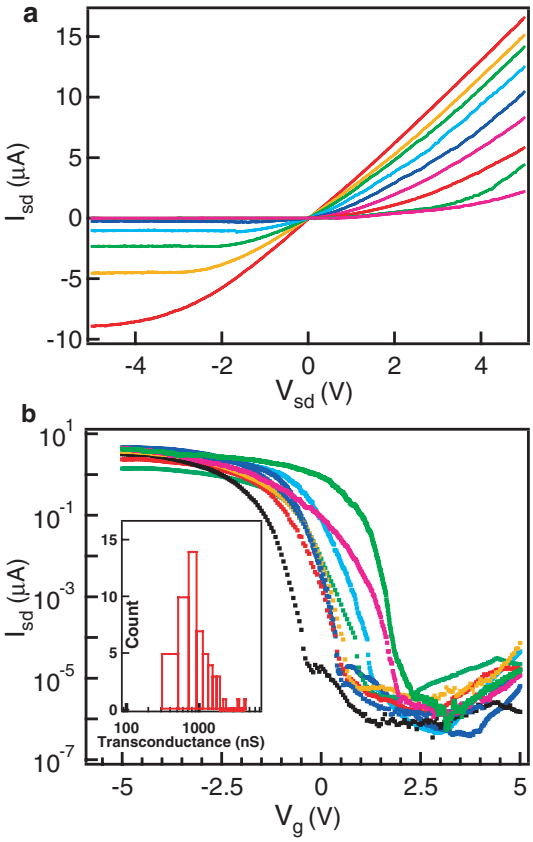

Fig. 8. (a) Family of source-drain current (I_{sd}) vs source-drain voltage (V_{sd}) plots at different gate voltages (V_g) for a typical device in the array; V_g varies from −5 (red) to +3 V (magenta). (b) I_{sd} vs V_g plots at a V_{sd} of 1 V for a sampling of devices from the large arrays; (inset) Histogram of the transconductance values observed for a sampling of devices in the large-scale array.

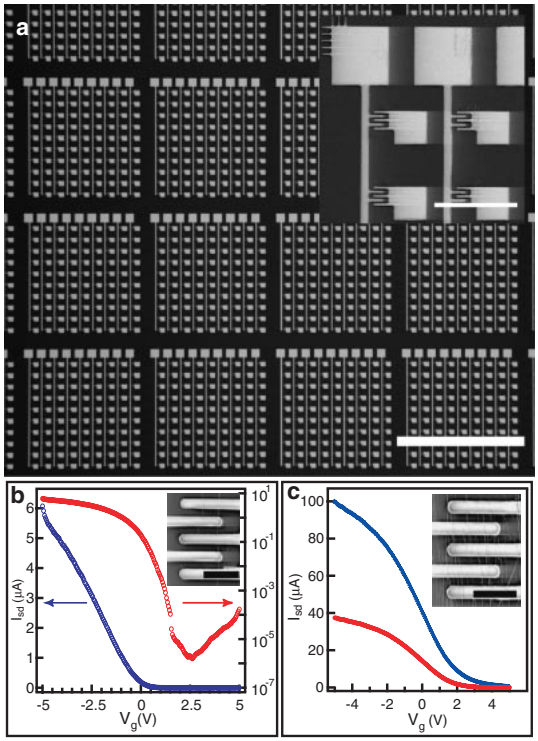

Fig. 9. (a) Optical micrograph of large-scale pixel-like electrode arrays deposited on hierarchically patterned NW arrays. Scale bar, 1 mm. (inset) SEM image of several device units fabricated on the patterned NWs. Scale bar, 100 μm. (b) I_{sd} vs V_g plots at a V_{sd} of 1 V for a typical device bridged with a low-density of aligned NWs; (inset) SEM image of a typical low-density NW device with about two aligned NWs bridging the interdigitated electrodes. Scale bar, 10 μm. (c) I_{sd} vs V_g recorded at a V_{sd} of 1 V (red) and 4 V (blue) for a typical device bridged with a high-density of aligned NWs; (inset) SEM image of a typical high-density NW device with about nine bridging NWs. Scale bar, 10 μm.

NW devices since there are ca. 6 times more active devices (35 vs 6) in the high versus low density arrays, respectively. In addition, a histogram of the threshold voltages determined from measurements on a large number of devices, exhibits a mean of 1.04 V and standard deviation of 0.36 V. This relatively narrow distribution is promising for applications, where uniformity of device characteristics is important.

6. Summary and Perspectives

We have outlined a general strategy for hierarchical assembly of NWs into integrated device arrays. Overall, our parallel and scalable approach enables NWs to be aligned with controlled pitch and hierarchically assembled into repeating arrays, in which the specific NW building blocks, NW pitch, NW orientation, array size, array orientation, and array pitch can be controlled independently. We have also demonstrated that the hierarchical assembly approach can be readily applied to the fabrication of large-scale arrays of high performance nanowire FETs with high reproducibility and scalability. These highly reproducible nanowire device arrays could be of great interest in a number of applications, including multiplexed chemical and biosensors[21] and information displays.[36] In this latter 'macroelectronic' application, a distinct advantage of our approach compared to those using high-performance thin-film devices is the room temperature processing, making it compatible with low-cost and flexible glass and plastic substrates.[37] More generally, this solution-based "bottom-up" assembly approach could enable facile integration of diverse NW building blocks with more complex structural hierarchy and flexible electrode designs, and thus provide a pathway for the assembly of a broad range of integrated functional nanosystems. We believe, for example, that crossed NW arrays could be readily implemented to yield addressable nanoscale light-emitting diode arrays and highly integrated logic/memory arrays that are needed for nanocomputing.[38]

Acknowledgments

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