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2002  November

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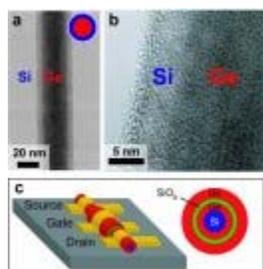
### Scientists shell out on nanowires

8 November 2002

**Researchers from Harvard University, US, have used chemical-vapour deposition to grow multiple shells around nanowires of silicon and germanium. Charles Lieber and his team also demonstrated a field-effect transistor based on a nanowire with a silicon core coated with layers of germanium and silicon oxide.**

"Building additional functionality into nanowires during synthesis enables new device architectures," team member Lincoln Lauhon told *nanotechweb.org*. "The method that we have described is very general and can be applied to a range of materials systems to enhance the performance of functional nanostructures."

To create the nanowires, the researchers began by depositing material onto nanocluster catalysts. The diameter of the resulting wires depended on the size of the nanocluster. Changing the growth conditions so that atoms could also deposit round the circumference of the nanowire - rather than just near the catalyst - produced a shell round the core. And introducing further reactants allowed the scientists to build up multiple shells.



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For example, Lieber and his team used gold nanocluster catalysts to grow nanowire cores of intrinsic silicon (i-Si) from silane gas. Then they added diborane to the mixture, which turned on radial shell growth and created a boron-doped p-type silicon (p-Si) shell round the intrinsic silicon core. The researchers also found that adding oxygen could oxidize an intrinsic silicon core, producing a thin amorphous layer of SiO<sub>x</sub>.

The scientists were able to grow boron-doped p-Si shells onto single crystal germanium (Ge) cores as well as deposit germanium coatings onto silicon nanowires. They also made a core-double-shell structure consisting of a 20 nm-diameter silicon core coated with a 30 nm layer of germanium and an outer shell of p-Si that was 4 nm thick.

Finally, the scientists made a coaxially gated nanowire field-effect transistor (FET). At the heart of the device was a core-multishell structure consisting of p-Si/i-Ge/SiO<sub>x</sub>/p-Ge. The i-Ge shell acted as the active channel, while selective etching and metal deposition onto the inner i-Ge shell and outer p-Ge shell created the source, drain and gate contacts. The Harvard team claims that the device's performance is comparable to those of recently reported carbon-nanotube FETs, even though it has yet to be optimized.

"Based on continuing discussions with the Intel Novel Device Group, we are pursuing the integration of very-high-performance field-effect transistors with conventional semiconductor processing to produce advanced hybrid devices," added Lauhon. Lauhon says core-shell structures also have applications in nonvolatile random access memory and photonic devices.

The researchers reported their work in *Nature*.

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Liz Kalaugher is editor of *nanotechweb.org*.

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