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Nanodevice connections leap forward

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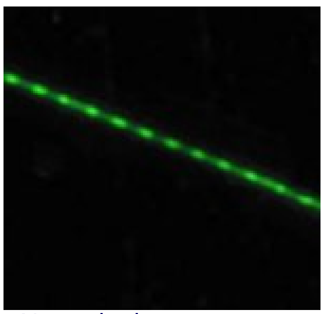
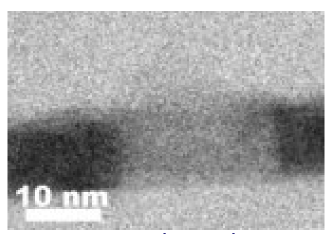
Until now, making contact to nanowires and nanotubes in electronic devices has meant using lithography to define metal electrodes. But this means that the contacts must be relatively large. Now, researchers at Harvard University, US, have come up with an integrated contact and interconnection method that overcomes this inherent size constraint. The technique transforms selected regions of silicon nanowires into metallic nickel silicide.


Nanowire heterostructure

"All previous studies of semiconductor nanowire/nanotube nanoelectronic devices have used lithographically defined metal contacts," Charles Lieber told *nanotechweb.org*. "This approach sets a size scale much larger than the nanowire/nanotube structures themselves (one defined by the same lithography used in industry), and thus precludes many advantages of the small size of nanowires. This motivated us to ask whether there were truly nanoscale solutions for contacting the nanowires that could be integrated ultimately on a large scale."

To make the contacts Lieber and colleagues laid down single-crystal silicon nanowires with diameters of about 20 nm by a chemical vapour deposition process using gold nanoclusters as catalysts. Then they deposited nickel onto the nanowires and heated them to 550°C so that they reacted to form nickel silicide. Finally the team removed the remaining nickel by wet etching.

The resulting single-crystal nickel silicide nanowires had low resistivities - about 10 microOhm cm - and failure-current densities greater than 10^8 A/sq. cm. The team has also prepared metallic single-crystal NiGe nanowires.



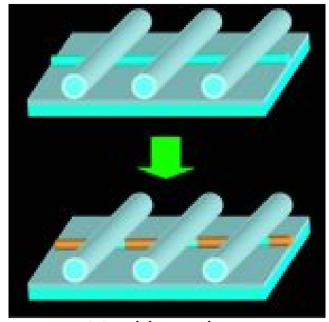
Integrated transistor

By treating only selected regions of a silicon nanowire, the researchers made heterostructures containing alternating 1 µm long areas of silicon and nickel silicide. Transmission electron microscopy showed that the interfaces between the two materials were atomically abrupt.

"These heterostructures have important implications in that they define integrated nanoscale transistors, and do so with metal/semiconductor contact defined with atomic precision for the first time," said Lieber. "This latter point is really quite important since [making] contacts to nano or molecular structures has been one of the least well-defined areas, yet is central to any future technology. For the first time we now have an approach to make the same atomically defined contact every time."

In this way, the team made a field-effect transistor in which the source-drain

regions were defined by nickel silicide sections on a p-type silicon nanowire. The researchers also used arrays of crossed nanowires as masks for defining active channels in nickel silicide/silicon/nickel silicide heterostructures.


Masking wires

"We showed a novel nanowire-based shadow masking method that can produce semiconducting silicon devices with a gate length as small as 10 nm seamlessly interconnected to metallic nickel silicide nanowire interconnects," said Lieber. "This is a critical step toward large-scale dense nanocircuit arrays, and also testing the fundamental performance limits of nanowire devices."

The researchers reported their work in *Nature*.

About the author

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