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Scalable Interconnection and Integration of Nanowire Devices without Registration

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ABSTRACT

A general strategy for the parallel and scalable integration of nanowire devices over large areas without the need to register individual nanowire–electrode interconnects has been developed. The approach was implemented using a Langmuir–Blodgett method to organize nanowires with controlled alignment and spacing over large areas and photolithography to define interconnects. Centimeter-scale arrays containing thousands of single silicon nanowire field-effect transistors were fabricated in this way and were shown to exhibit both high performance with unprecedented reproducibility and scalability to at least the 100-nm level. Moreover, scalable device characteristics were demonstrated by interconnecting a controlled number of nanowires per transistor in "pixel-like" device arrays. The general applicability of this approach to other nanowire and nanotube building blocks could enable the assembly, interconnection, and integration of a broad range of functional nanosystems.

Semiconductor nanowires (NWs) and carbon nanotubes (NTs) have been used as building blocks for fabricating a wide range of nanoelectronic and nanophotonic devices,[1−3] including field-effect transistors (FETs),[4−7] light-emitting diodes,[6,8,9] and diode lasers.[10] Developing integrated nanoelectronic and nanophotonic systems utilizing the diverse properties of NWs and NTs will require techniques that can assemble these building blocks in a parallel, scalable, and highly reproducible manner independent of the specific materials. Studies involving fluidic[11] and electric field-directed[6,12,13] assembly have shown the potential of manipulating these building blocks from solution yet have realized only relatively small scale structures. Approaches that are fully scalable in terms of device density and area of coverage have not been reported, despite their central importance to the development of the bottom-up assembly of nanosystems.[1,14,15]

Here we describe a strategy that enables the parallel and scalable integration of NW devices over large areas without the need to register individual nanowire−electrode interconnects. We implemented this approach using a Langmuir−Blodgett method to organize NWs with controlled alignment and spacing over large areas[16] and parallel photolithography to define interconnects in a statistical manner. Centimeter-scale arrays containing thousands of silicon NW FETs fabricated in this way were shown to exhibit high performance with unprecedented reproducibility and scalability to at least the 100-nm level. The general applicability of this approach to a wide range of NW materials and organized NW structures could enable a pathway to highly functional and integrated nanosystems.

Our approach to large-scale and parallel interconnection exploits the fact that the separation between NWs assembled by the Langmuir−Blodgett method[16] has a defined average value but varies on the local scale. In this context, it is possible to achieve a high yield of metal electrode-to-nanowire contacts simply by setting the average NW separation equal to a value comparable to the electrode width (Figure 1a); that is, the local fluctuations in separation lead to an efficient formation of contacts. This approach includes the following steps (Figure 1b): First, a uniform parallel layer of aligned NWs with a controlled average spacing is transferred to a substrate surface from NWs that are uniaxially aligned at the air−water interface on a Langmuir−Blodgett trough (inset, Figure 1b).[16] Then the uniform NW layer is hierarchically patterned into parallel NW arrays by photolithography, where NWs are removed from regions outside of the defined pattern. Finally, large-scale device arrays are fabricated by defining complementary electrode arrays. There are two key features in this approach. First, it

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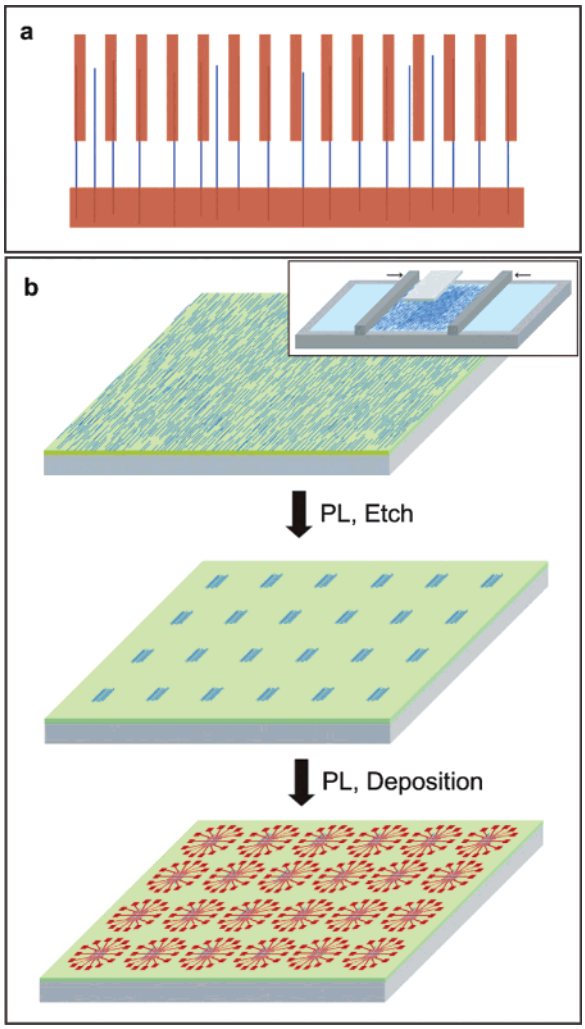

Figure 1. Parallel and scalable interconnection of NW devices without registration. (a) Central electrode region of a single array emphasizing the high fraction of interconnected NWs (blue lines) obtained without the registration of individual electrodes. (b) Schematic illustrating key steps of the interconnection approach, including (top) the deposition of aligned NWs with defined average spacing over the entire substrate, (middle) hierarchical patterning to produce fixed size and pitch parallel NW arrays, and (bottom) the deposition of a repeating metal electrode array using photolithography (PL).

is not necessary to register the metal electrodes, which are defined by conventional lithography, to individual NWs in an array to achieve a high yield of contacts; only the position of the electrodes relative to a group of aligned NWs needs to be fixed. Second, the approach is intrinsically scalable to large areas because each of the key steps (Figure 1b) can be carried out over an entire substrate or wafer in parallel.

We first illustrate our approach with the fabrication of large arrays of NW FETs in which each active device consists of a single p-type silicon NW.[17,18] In general, the NW arrays were made on 1−10 cm^2 substrates as described previously,[16] and then in the final metal electrode deposition step, the photolithography mask was aligned only to the position of the repeating NW arrays.[19] Optical and electron microscopy images (Figure 2a−c) demonstrate the key features and

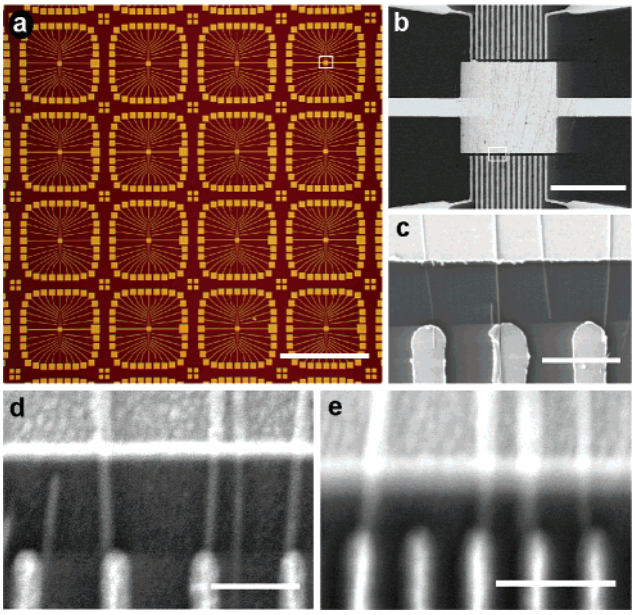

Figure 2. (a) Optical micrograph of integrated metal electrode arrays deposited on top of patterned parallel NW arrays defined by photolithography. Scale bar, 1 mm. (b) Scanning electron microscope (SEM) image of the central active region of a repeat unit of the electrode array shown in part a. Scale bar, 40 μm. (c) SEM image of three NW devices connected between the common and finger electrodes. Scale bar, 3 μm. (d, e) SEM images of higher-density NW devices defined by electron beam lithography. Scale bars, 300 nm.

hierarchy of structures produced by our approach, including (1) FET subarrays with a 1-mm array pitch repeated over the entire substrate (Figure 2a), (2) central electrode arrays on a 3-μm electrode pitch (Figure 2b), and (3) individual 20-nm-diameter NWs connected between the finger electrodes and the common electrode (Figure 2c). Figure 2c also illustrates that single NWs can fall between two metal electrodes as expected statistically, although the overall NW alignment prevents such "defective devices" from adversely affecting properly interconnected NWs. Using this method, approximately 80% of the 3000 possible electrode connections available on a typical test chip could be bridged by NWs when the spacing of the aligned NWs was closely matched to the electrode width (ca. 1 μm in this demonstration). The average nanowire spacing can be reduced further to increase the connection yield, although this also increases the probability of having multiple nanowires connected to one electrode. (See below.) Significantly, the large scale over which device arrays are produced by our alignment and patterning technique greatly exceeds that of previous studies.[6,11−13]

Our basic approach is scalable and thus can be used to produce devices in the nanometer size regime over large areas. Because the average NW spacing can be controlled down to the nanometer scale during the Langmuir−Blodgett compression,[16] a much smaller device size and a higher density of device integration can be readily achieved when existing high-resolution parallel lithography techniques, such as submicrometer photolithography, extreme-UV lithography,[20] or nanoimprint lithography,[21] are applied to define

electrodes following this interconnection strategy. To demonstrate this key point of scaling, we have used electron beam lithography to define regular nanometer-scale contact electrodes without registering them to individual NWs.[19] Notably, electron microscopy images show clearly that individual NWs are connected in high yield for electrodes with 300-nm (Figure 2d) and 150-nm (Figure 2e) pitch. There are also NWs that fall between the electrodes, as expected statistically, although these are not expected to affect the interconnected active devices.

The electrical characterization of randomly chosen NW devices within the large arrays (Figure 3a) shows linear source−drain current (I_{sd}) versus source−drain voltage (V_{sd}) curves for small V_{sd} and saturation at larger negative voltages as expected[22] for p-type field-effect transistors. A linear plot (Figure 3b) of I_{sd} versus gate voltage (V_g) yields a peak transconductance, dI_{sd}/dV_g, of ca. 1250 nA/V, and a logarithmic plot (Figure 3b) demonstrates an on/off current ratio and a subthreshold slope of ca. 7×10^6 and 160 mV/decade, respectively. The increase in I_{sd} for $V_g > 2.5$ V is believed to be due to gate leakage. Moreover, studies of a large number of devices show that these results are reproducible. I_{sd} versus V_g plots for nine devices (Figure 3c) all exhibit on/off current ratios greater than 10^6 and substhreshold slopes below 250 mV/decade, where the highest on/off ratio is 10^7 and the lowest substhreshold slope is 140 mV/decade. A histogram of the observed peak transconductance values for these and many other devices (Figure 3c inset) shows a most probable value close to 1000 nA/V and a maximum value of 4300 nA/V corresponding to a calculated hole mobility of 307 $cm^2/V \cdot s$. These results demonstrate that the solution-based assembly does not adversely affect the performance or reproducibility of the NW devices.

The observed reproducibility of these NW transistors suggests that our approach could be used as a general route for assembling and investigating the properties of large-scale integrated systems in which NWs serve as key functional elements. To this end, we have fabricated pixel-like arrays (Figure 4a) in which interdigitated electrodes were used as contacts to the patterned NWs. A unique feature of this electrode scheme is that the number of NW devices per "pixel transistor" can be readily varied by controlling the NW spacing[16] prior to the deposition of the contact electrodes. If the NW devices behave reproducibly, then it should be possible to scale key device characteristics, such as the transistor on current, simply by controlling the number of NWs contacted by the interdigitated electrodes at a given pixel-like device element.

The transfer of aligned NWs with a relatively large, 6-μm average spacing yielded only a few NWs bridging each set of interdigitated electrodes (inset, Figure 4b). The I_{sd} versus V_g plots (Figure 4b) display an on current of ca. 6 μA and an off current of ca. 1.6 pA at V_{sd} values of 1 V, with an on/off current ratio of ca. 4×10^6 and a transconductance of 1400 nA/V. Device elements fabricated using NW arrays with a smaller average NW spacing of ca. 1 μm yielded multiple NWs bridging the interdigitated electrodes (inset, Figure 4c). Representative I_{sd} versus V_g data recorded from

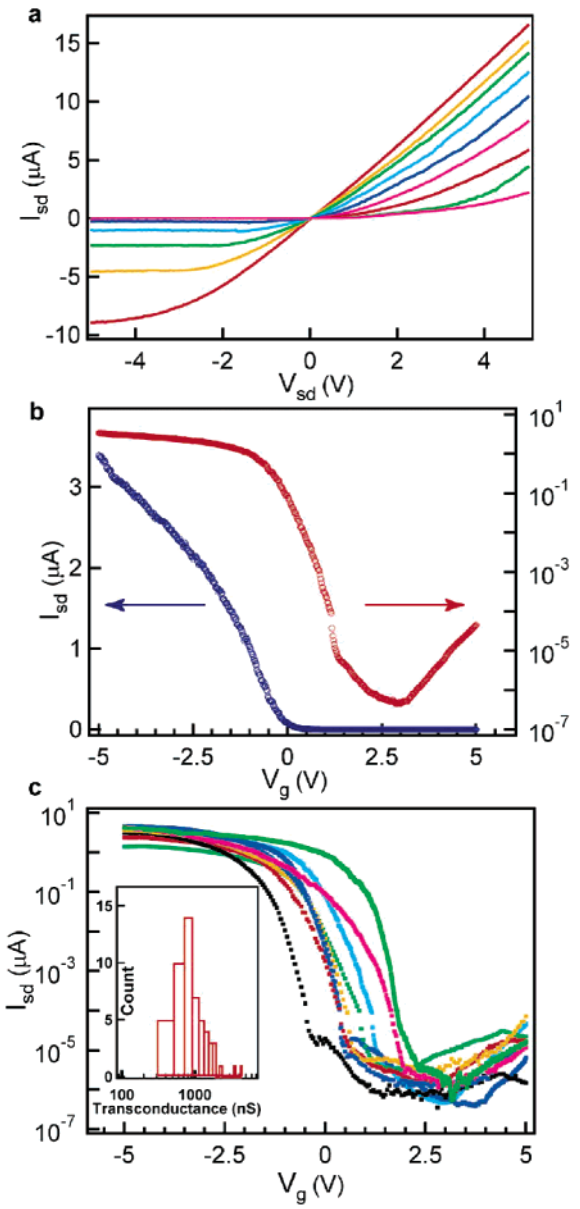

Figure 3. (a) Family of source−drain current (I_{sd}) vs source−drain voltage (V_{sd}) plots at different gate voltages for a typical device in the array. The red, orange, green, cyan, blue, magenta, red, green, and magenta curves correspond to V_g values of −5, −4, −3, −2, −1, 0, 1, 2, and 3 V, respectively. (b) I_{sd} vs gate voltage (V_g) recorded for a typical device plotted on linear (blue) and log (red) scales at a V_{sd} of 1 V. (c) I_{sd} vs V_g plots at a V_{sd} of 1 V for a sampling of devices from the large arrays. (Inset) Histogram of the transconductance values observed for a sampling of devices in the large-scale array.

one set of electrodes (Figure 4c) show on currents of ca. 37 μA at a V_{sd} of 1 V and 100 μA at a V_{sd} of 4 V in the regime near saturation. These currents are ca. 6 times the value observed for devices with lower NW densities (Figure 4b). Significantly, the differences in on currents demonstrate excellent scaling of properties in the multi-NW devices because there are ca. 6 times more active devices (35 vs 6) in the high- versus low-density arrays, respectively. In addition, a histogram of the threshold voltages (Figure 4d) determined from measurements on a large number of devices exhibits a mean of 1.04 V and a standard deviation of 0.36

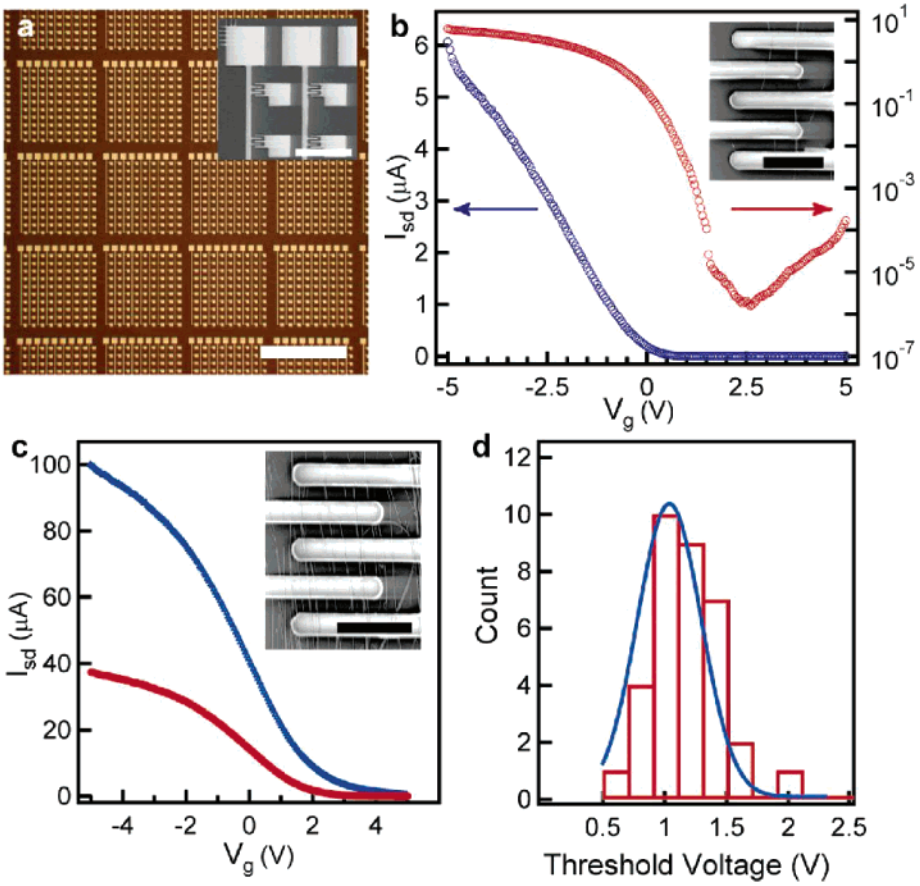

Figure 4. (a) Optical micrograph of large-scale pixel-like electrode arrays deposited on patterned parallel NW arrays. Scale bar, 1 mm. (Inset) SEM image of several device units fabricated on patterned NWs. Scale bar, 100 μm. (b) I_{sd} vs V_g recorded for a typical low-density NW device plotted on a linear scale (blue) and a log scale (red) at a V_{sd} of 1 V. (Inset) SEM image of a typical device with two aligned NWs bridging the electrodes. Scale bar, 10 μm. (c) I_{sd} vs V_g plots at $V_{sd} = 1$ (red) and 4 V (blue) for a typical device bridged with a high density of aligned NWs. (Inset) SEM image of a typical high-density NW device with about nine aligned NWs bridging the electrodes. Scale bar, 10 μm. (d) Histogram of the observed threshold voltages for the high-density NW devices; the solid line corresponds to a Gaussian fit.

V. This relatively narrow distribution is promising for applications where the uniformity of device characteristics is important.

These studies demonstrate a powerful strategy for the parallel and scalable interconnection of electrically addressable NW devices over large areas. We have shown that this approach can yield massive arrays of high-performance field-effect transistors with high reproducibility, and we believe that these highly reproducible transistor arrays could find uses in a number of applications ranging from multiplexed biosensing[23] to information displays.[24] In this latter "macroelectronic" application, a distinct advantage of our approach compared to those using high-performance thin-film devices[25] is the room-temperature processing, making it compatible with low-cost and flexible glass and plastic substrates.[26,27] In addition, it should be possible to exploit this approach to fabricate high-performance logic circuits in which NWs replace conventional single-crystal planar silicon devices because the NW devices assembled on a large scale in this work rival state-of-the-art planar devices.[28] Specifically, by introducing another step of photolithography and metal deposition, it will be possible to define the addressable gate electrodes required for logic circuits. More generally, our approach could be used to interconnect distinct types of parallel NWs and crossed NW arrays, enabling diverse electronic and photonic functionality using different NW building blocks.[1] This work thus provides a pathway for the development of highly functional and integrated nanosystems.

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(18) Single-crystal silicon nanowires were prepared with a SiH_4/B_2H_6 ratio of either 4000:1 or 8000:1 using 20-nm-diameter gold nanocluster catalysts.[17] Nanowires were aligned and then transferred[16] to degenerately doped (resistivity < 0.005 Ω·cm) silicon (100) substrates coated with 60-nm-thick sputtered ZrO_2 (Silicon Valley Microelectronics, Inc., San Jose, CA). Aligned nanowire layers were patterned by photolithography, and the nanowires outside the patterned areas were removed by sonication in deionized water.[16]
(19) Electrode interconnects to the patterned nanowire arrays were prepared by standard photolithography to define a repeating pattern, followed by the thermal deposition of Ni (70 nm). The high-resolution integrated electrode array patterns were defined by electron beam lithography, followed by the thermal deposition of Ni contacts. Electrical transport measurements were made at room temperature with a high-precision semiconductor analyzer (Aglient 4156C, Agilent Technologies, Palo Alto, CA) and a probe station (Desert Cryogenics, Tucson, AZ).
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