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Electrochemical Deposition of Conformal and Functional Layers on High Aspect Ratio Silicon Micro/Nanowires

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Supporting Information

ABSTRACT: Development of new synthetic methods for the modification of nanostructures has accelerated materials design advances to furnish complex architectures. Structures based on one-dimensional (1D) silicon (Si) structures synthesized using top-down and bottom-up methods are especially prominent for diverse applications in chemistry, physics, and medicine. Yet further elaboration of these structures with distinct metal-based and polymeric materials, which could open up new opportunities, has been difficult. We present a general electrochemical method for the deposition of conformal layers of various materials onto high aspect ratio Si micro- and nanowire arrays. The electrochemical deposition of a library of coaxial layers comprising metals, metal oxides, and organic/inorganic semiconductors demonstrate the materials generality of the synthesis technique. Depositions may be performed on wire arrays with varying diameter (70 nm to 4 μm), pitch (5 μ to 15 μ), aspect ratio (4:1 to 75:1), shape (cylindrical, conical, hourglass), resistivity (0.001−0.01 to 1−10 ohm/cm^2), and substrate orientation. Anisotropic physical etching of wires with one or more coaxial shells yields 1D structures with exposed tips that can be further site-specifically modified by an electrochemical deposition approach. The electrochemical deposition methodology described herein features a wafer-scale synthesis platform for the preparation of multifunctional nanoscale devices based on a 1D Si substrate.

KEYWORDS: *Core−shell structures, silicon nanowire arrays, electrochemistry, hybrid layers, one-dimensional structures, wafer-scale deposition*

Advances in nanoscience benefit from the development of methods for the synthesis of complex structures.[1−5] Fundamental light-matter interactions may be manipulated with the synthesis of well-defined one-dimensional (1D) nanostructures, which display novel sensing and light harvesting applications,[6−14] and the development of energy conversion devices[15−18] have been enabled by surface and architectural engineering of the chemical and physical properties of 1D materials.[12,19−22] In the field of medicine, nanoelectronic devices based on 1D Si nanowires have exhibited remarkable performance in bioelectronic and drug delivery applications.[23−28] Further applications of 1D materials could be broadened by synthetically elaborating these structures with distinct types of materials to yield complex compositions and architectures with enhanced or new functional properties.

Physical vapor deposition techniques operating under high vacuum are generally useful for the deposition of uniform films on flat substrates but cannot be used to elaborate nonplanar structures with uniform thickness because they operate with line-of-sight deposition.[29] Sputter deposition can overcome some challenges in deposition on nonplanar structures, although it remains limited in application for high-density arrays and/or high aspect ratio structures.[29] Atomic layer deposition (ALD) can produce uniform 3D conformal films,[30] although constraints of reactants and deposition conditions[31,32] necessary to meet ALD limit its usage for many classes of interesting materials, including organics,[33] and for preparation of thicker layers needed for many applications.

Electrodeposition represents an alternative and powerful approach for deposition of films on flat substrates[34−38] and has shown promise for deposition of nanoparticles[39−41] and thin shells around 1D nanostructures;[42−45] however, the approach has yet to be exploited as a general synthetic methodology for modifying micro- and nanowire structures with uniform shells of a broad range of materials or to prepare multiple coaxial shell layers. Here, we present a rapid, ambient temperature solution-phase electrodeposition method for conformal and uniform deposition of a large variety of materials on these high aspect ratio 1D structures. To demonstrate the materials generality of this synthesis approach, a selection of catalytically, magnetically, and plasmonically active metals (Au, Ag, Cu, Pt, Pd, Ru, Rh, Ni, Fe), catalytic metal oxides (MnO_x, CoO_x), semiconducting metal chalcogenides (CdS, CdSe), and conductive polymers (polyaniline, polypyrrole, poly-3,4-ethylenedioxythiophene) have been deposited on 1D high-aspect ratio Si micro- and nanowire structures. Conformal depositions have been

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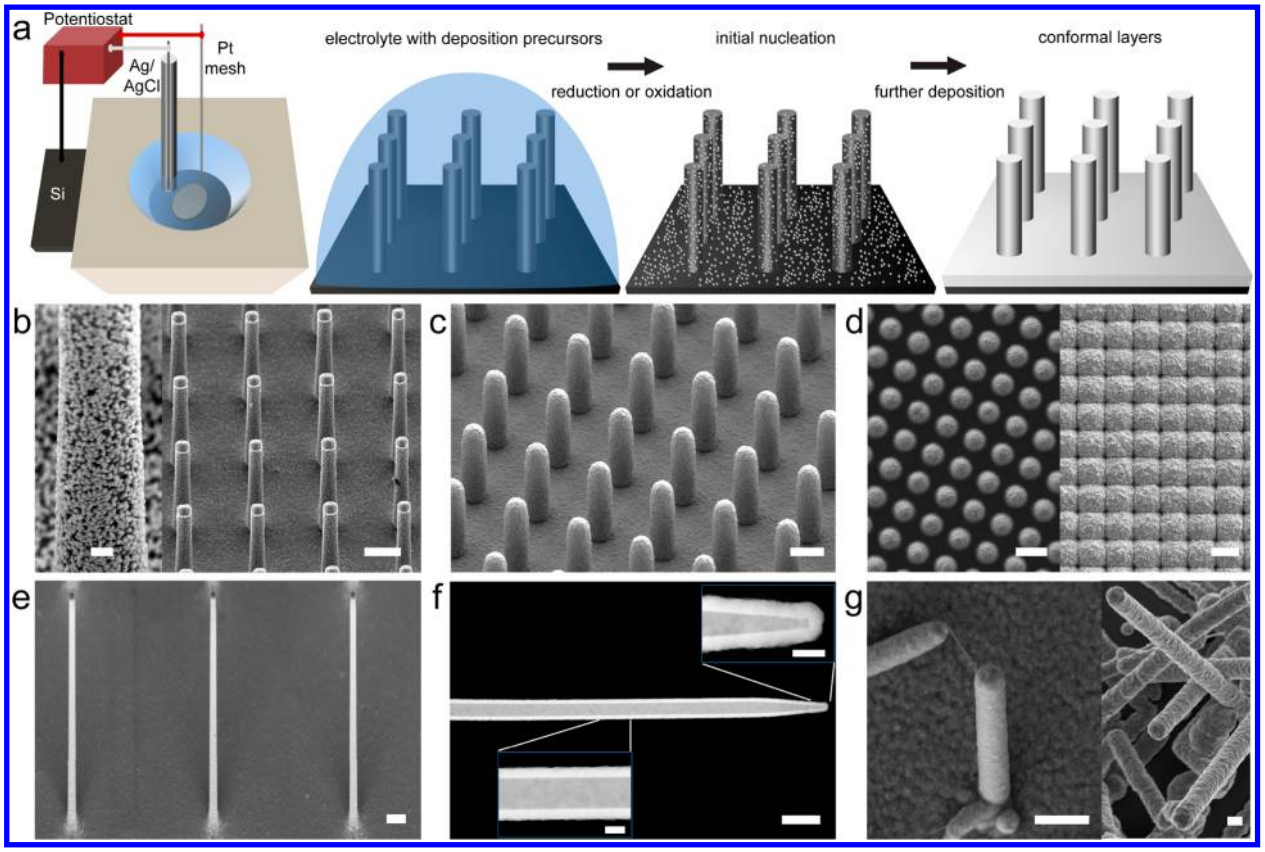

Figure 1. Electrodeposition of materials on micro/nanowires. (a) Schematic depicting the experimental setup and different stages of the electrodeposition process. SEM images of (b) Ni nanoparticles (left image is a zoomed in image of the wire), (c) a Ni layer in tilt-view from the middle of the array. (d) Top-view SEM images show progressive Ni deposition over time with reductive deposition. For the deposition on high aspect ratio structures, SEM image of (e) Ni covered top-down fabricated Si nanowires and (f) STEM for detailed characterization of film uniformity (insets are zoomed in images of the wire tip and wire body), and SEM images of (g) isolated and dense arrays of bottom-up grown Si nanowires with Ni layers. Scale bar equals 5 μm (inset 500 nm) for (b), 5 μm for (c,d), 2 μm for (e,f) (inset 200 nm), and 2 μm and 200 nm for (g).

optimized on high aspect ratio structures embedded in a photoresist matrix to assess both the compatibility of the technique with semiconductor processing and the possibility of site-selective deposition on the structures.

Vertically oriented Si micro- and nanowire arrays were chosen as substrates as the periodicity and aspect ratio of the wires can be precisely defined in the photolithography and reactive ion etching steps of a standard top-down nanowire fabrication process, as detailed in the Supporting Information.[46,47] Briefly, SU-8 negative photoresist (MicroChem) was spun cast at 3000 rpm for 1 min on Si substrates and prebaked at 65 and 95 °C for 2.5 and 5 min, respectively. The 1.5−2 μm diameter dot patterns were defined on the substrates using a mask aligner for 20 s exposure followed by 1 min developing in SU-8 developer solution. The photoresist pattern was postbaked at 180 °C for 20 min. The wire arrays were formed under a cyclic deep reactive ion etching process (SPTS Technology) and the length of the wires were controlled with the number of cycles (200−800 cycles). Diameter of the wires were controlled by growing a thermal oxide layer around the microwires at 1000 °C in a wet oxide furnace (1−8 h depending on the desired diameter) and subsequent etching of the oxide layer in 7:1 buffered oxide etch solution (J.T. Baker) for 1 h. In a typical electrodeposition experiment, Si wire arrays are covered via electrochemical oxidation (for polymers and oxides) or reduction (for metals) in a Teflon cell using a conventional three-electrode (Ag/AgCl reference, Pt counter, and Si working) setup connected to a potentiostat as depicted schematically in Figure 1a. Details of the precursor solutions and deposition parameters are given in Supporting Information, and SEM images of bare wire arrays, photographs of the deposition cell, and metal-deposited samples are presented in Figures S1−S4. Electrolyte solutions comprising either organic monomers or metal ions completely cover the substrate surface where nucleation sites eventually evolve to thin films around wire constructs under constant potential application (Figure 1a). Morphology and thickness of the resulting film can be controlled with the deposition time, which corresponds to the amount of charge passing into solution. To demonstrate the viability of this approach different metals were deposited on micro- and nanoscale wires with varying pitch, aspect ratio, and resistivity. For example, Si wire arrays fabricated from ∼1−10 ohm/cm^2 resistivity substrates are homogeneously decorated with Ni nanoparticles at an applied potential of E_{appl} = −0.9 V (all potentials are reported versus Ag/AgCl reference electrode unless stated otherwise) from a nickel sulfamate solution (Technic High Speed Nickel Sulfamate FFP RTU solution, containing 30% nickel sulfamate, 3% boric acid, 0.7% nickel bromide) within 10 min as depicted in the scanning electron microscope (SEM, typically recorded at 3 kV using in-lens and Everhart-Thornley detectors) images in Figure 1b. Likewise, Au nanoparticles are uniformly nucleated on Si wire arrays (Figure S5a) at E_{appl} = −0.93 V from a gold cyanide solution (Technic Orotemp 24 RTU, 1% potassium aurocyanide). Further

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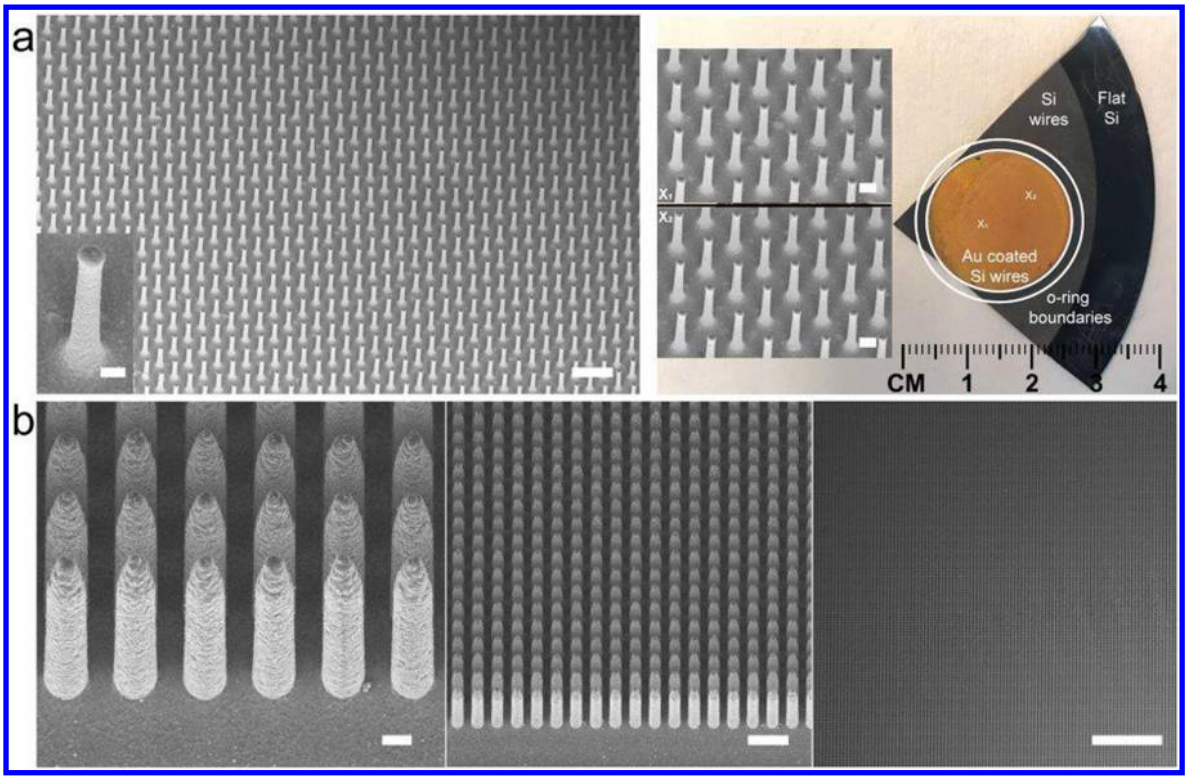

Figure 2. Scalability of deposition. An array of Au-covered Si wires imaged with (a) SEM (inset is a zoomed in image of the wire) on the left for microscale analysis at high magnification and photograph on the right for macroscale comparison with a virtual ruler (insets are SEM images recorded from the points marked with "X_1" and "X_2" in the photograph). (b) Cross-sectional view of a polymer layer covered wire array with textured tips and a dense pitch, images of the array were recorded at decreasing magnifications from left to right for larger area view for confirming the uniformity and scalability of the deposition method. Scale bar equals 10 μm (inset 1 μm) and 4 cm (insets 2 μm) for (a); and 2, 10, and 100 μm for (b).

deposition ultimately leads to merging of nanoparticles into a conformal film on the surface of the wires (Figure S5b). The rate of deposition is measured to be higher in more conductive samples as the flux of charge passing through the electrodes is inversely correlated with the resistivity of the substrate. For instance, Si wire arrays prepared using ~0.001−0.01 ohm/cm^2 substrates are covered with a homogeneous thick layer of Ni with E_{appl} = −0.9 V in as little as 5 min (Figure 1c). SEM images were taken by tilting the sample 30° along their long axis to observe the uniformity of the deposition from bottom to top and to determine the extent of cross-deposition between the wires, particularly at the edge of the wire arrays (Figure S6). A thickness progression over time has been studied on an array with a moderate wire-to-wire spacing (~10 μm) (Figure 1d, left). Deposition is stopped after the gap between the nanowires is completely filled and all wires are buried under a layer of continuous metal film (Figure 1d, right). Inside-out progression of the layers around the wires demonstrates the utility of this method in conformal deposition and its potential for preparing coaxial devices. For samples with lower conductivity, increasing the charge flux by increasing E_{appl} to −1.3 V is also found to deposit a layer of metal on the Si surface rapidly. Although the resistivity of Si has a significant impact on the formation of metal films during the reduction process, the oxidation process is found to be less sensitive to resistivity. For instance, similar quality polymer films were achieved under +1.0 V constant potential deposition on both low (Figure S7a, polyaniline deposited from 680 μL aniline in 15 mL of 0.1 M $LiClO_4$) and high resistivity substrates (Figure S7b, polypyrrole deposited from 510 μL pyrrole in 30 mL of 0.1 M $HClO_4$). This is most likely due to one to two orders of magnitude higher concentrations of organic monomers relative to the typical concentration of metal ions in electrolytes used in depositions.

To test the feasibility of this technique for use with very high aspect ratio 1D nanostructures, ~25 μm long Si nanowire arrays with 330 nm diameter (aspect ratio of 75:1) were covered with a thin layer of Ni. Both SEM images in Figure 1e and Figure S8 and scanning transmission electron microscope images in Figure 1f (STEM at 200 kV in the Z-contrast dark-field mode) confirm the conformal deposition of the Ni-shell layer with good uniformity and high fidelity. The morphology of the layer deposited on the 1D nanowire array is similar to that of layers deposited on the planar surface of the silicon substrate (Figure S6). For a more detailed characterization, wires were removed from the substrate and then transferred onto TEM grids. STEM analysis clearly differentiates the core and shell materials based on atomic number such that Si appears in dark contrast and Ni appears in bright contrast (Figure 1f, Figure S9). The diameter of the Si core at the body of the wire is 330 nm ± 2 nm and the conformal Ni shell around is 98 ± 8 nm thick film. We observe that the deposited shell follows the geometry of the wire as it tapers toward the tip. The tip of the Si core is 65 ± 2 nm with a conformal shell thickness of 86 ± 13 nm.

The deposition methodology was also tested on very thin bottom-up grown nanowires oriented in random directions. These wires were synthesized using the conventional nano-cluster-catalyzed vapor−liquid−solid technique.[22] Briefly, 5 mL of solution of 100 nm Au nanoparticles was mixed with 0.5 mL

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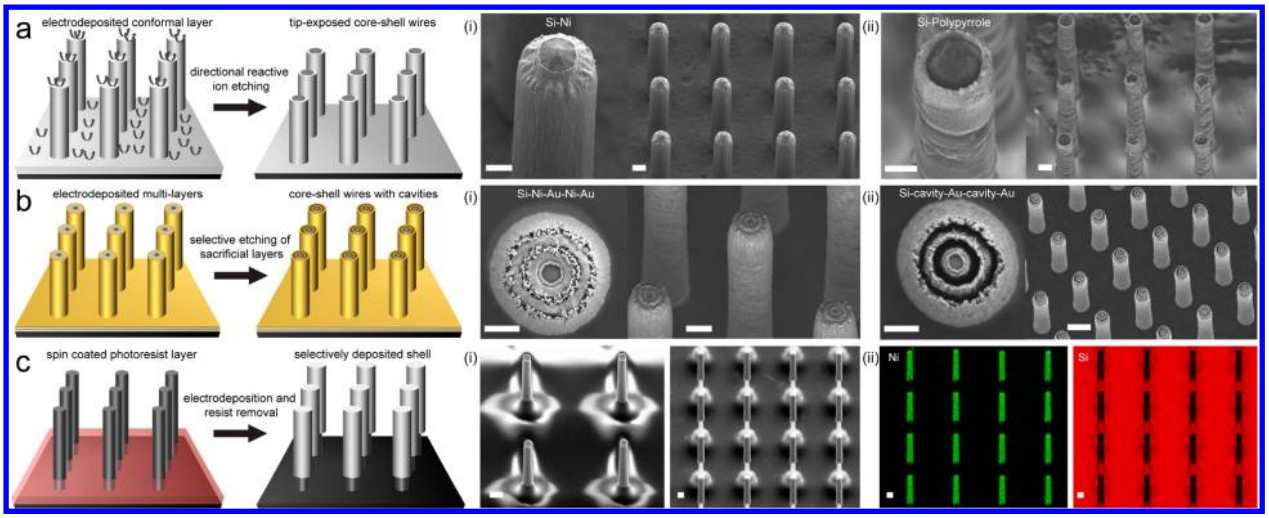

Figure 3. Structural design and site-selective deposition. (a) Schematic representation of the directional reactive ion etching process for the exposure of the tips of the wires. Electron microscope images of Si core (i) Ni shell, (ii) polypyrrole shell nanowires confirm the coaxial nature of the deposition and exposes the tips of silicon for future modifications. (b) Schematic representation of multilayer deposition and selective removal of sacrificial layers. SEM images of Ar plasma etched Ni−Au−Ni−Au coaxial multimetallic Si nanowires (i) before and (ii) after selective etching of sacrificial Ni layers confirm the presence of cavities in between Si wire and the Au shells. (c) Schematic representation of site-selective deposition by masking the surface of the substrate and the lower portion of the wires with a photoresist layer. Electron microscope images of Si core (i) with a photoresist layer (left) and after deposition of Ni layers (right), (ii) corresponding elemental maps for Ni (left) and Si (right) confirm selective deposition only at the photoresist free nanowire body. Scale bars for the magnified images on the left panel of each subfigure for (a) and (b) equal 1 μm; the right panel of (a−c) is 2, 2, 2, and 5 μm, respectively. Scale bar equals 2 μm for (c).

of 49% HF solution and dispersed on Si substrates to serve as the catalyst for the growth of Si nanowires in a home-built chemical vapor deposition reactor. Nanowire growth was carried out for 30 min at 475 °C at a total pressure of 10 Torr with 1 standard cubic centimeter per second (sccm) silane, 60 sccm hydrogen, and 3 sccm diborane flow rates (see the Supporting Information for further details). SEM images in Figure 1g confirm that the electrodeposition occurs on the conductive nanowire surface and a conformal Ni shell grows coaxial to the nanowire orientation. The uniform shape of the shell layer suggests that the solution-phase electrochemical deposition does not have a noticeable facet-dependency for nanowires with sub-100 nm diameters.

Scalability of this approach is tested for both the reduction and oxidation processes (Figure 2). Figure 2a illustrates a large-scale array of nanowires with an electrochemically deposited Au shell recorded at high magnification using an electron microscope (left) and without magnification using a conventional camera (right). SEM images taken from various spots on the nanowire array confirm the uniformity of the deposition through the array (Figure 2a insets and S10). Moreover, we observed that our method is highly tolerant to imperfections on the wire surface and differences in wire dimensions. For example, nanowires with textured tips were uniformly covered with a layer of polypyrrole. The corresponding wire images before (Figure S11) and after deposition are presented in Figure 2b. Zoomed out SEM images (Figure 2b left to right) illustrate the uniformity of the deposition across the sample and the scalability of this approach. This sample confirms that even in a dense array of wires with a narrow pitch (~5 μm), all wires, including those at the edge of the array, have well-isolated conformal layers. The deposition method was also tested on a wire array consisting of cone-shaped short wires and hourglass shaped tall wires (Figure S12a,b). A conformal layer of Ni was deposited by preserving the morphology of the wires after deposition as depicted in Figure S12c suggesting the applicability of the method on arbitrary structures.

Our method provides another handle with which to control site-selective functionalization and structural design of nanowires. Tip modifications of the nanowires can be accomplished with reactive ion etching (RIE). In an optimized RIE process using directional argon plasma (10 min physical etching with 20 sccm of Ar flow and 400 W of applied DC power and 200 W of applied RF power at 5 mT pressure), the tips of the wires are anisotropically etched as depicted schematically in Figure 3a. For example, Ni and polypyrrole covered wires after RIE etching are shown in Figures 3a (i) and (ii) in which argon plasma has physically removed the top portion of the wires, resulting in core/shell wire architectures with exposed tips. Because the shell layer masks the outer part of the wire, this approach allows for tip selective functionalization of these Si nanowires. In terms of architectural control, more complex core/shell nanowire structures may be prepared through the use of sacrificial layers that can be etched selectively as depicted schematically in Figure 3b. In this regard, alternating depositions of Ni and Au layers yields the multishell structure shown in Figure 3b (i) post-tip etching. Selective wet etching of Ni (in 3% w/w aqueous solution of $FeCl_3$ for 60 min) then yields a core/shell structure with two Au satellites surrounding a Si nanowire as shown in Figure 3b (ii). The spacing between the Si core and the coaxial shells may be backfilled with a material of interest or may be used as a dielectric (air) in optical and electrical device applications. Compatibility of the method with semiconductor manufacturing organics and the possibility of site-selective deposition was assessed with a widely used photoresist Microposit S1818 (MicroChem) as schematically depicted in Figure 3c. This photoresist was dispensed on the Si wire array and the sample was spun at 2000−3000 rpm for 1 min to achieve a uniform layer (1−2 μm) on the Si substrate. The photoresist film masks only the base of the wires while leaving the rest of the wire exposed (Figure 3c (i)). In this case,

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electrodeposition takes place only at the conductive nanowire surface. Using the photoresist masking approach, Au and Ni layers were deposited on the wires while leaving the lower part of the sample bare (Figures 3c (i) and S13). SEM analysis and elemental maps (dispersive X-ray analysis was done at 15 kV) recorded after dissolution of the photoresist in acetone confirm the selective deposition on the exposed sites (Figure 3 (ii) for Ni). An SEM image and its corresponding elemental map for a masked and an unmasked nanowire array covered with Au are presented in Figure S14 for comparison purposes.

Optimization of material concentration, deposition potential, and substrate resistivity parameters allows the method to be generalized to different material classes including conductive polymers, other metals, metal oxides, and inorganic semiconductors (experimental details for deposition of 18 different materials on Si wires are detailed in the Supporting Information). An exemplary material from each class is presented with Rh in Figure 4a, polyaniline in Figure 4b, Mn_xO_y in Figure 4c, and CdSe in Figure 4d. Large area images of the single wires modified with more materials are presented with Ag in Figure S16, CdSe and CdS in Figure S17, Rh and Ni−Ru in Figure S18, along with close-up images of Cu-, Pd-, Fe-, and Pt-modified wires in Figure S19. For the construction of multicomposition systems, different materials were deposited consecutively. In one example, a hybrid structure made of a Si core covered with a Ni inner shell (deposited at $E_{appl} = -0.9$ V) and a polyaniline outer shell (polymerized at $E_{appl} = +1.0$ V) is shown in Figure 4e. In another example, a bimetallic structure made of a Si core covered with a Ni inner shell (deposited at $E_{appl} = -0.9$ V) and a Ru outer shell (deposited at $E_{appl} = -1.0$ V) is shown in Figure 4f and Figure S18b. These samples show that sequential depositions of various materials are possible as long as the surface that is in contact with the electrolyte is conductive. A special case in which a bubble forms at the electrode surface and consequently leaves the wires under the bubble unmodified is presented in Figure S20. Schematic representation, STEM analysis, and elemental maps (dispersive X-ray analysis was done at 200 kV) of a Si−Ni−Au coaxial wire are presented in Figure 4g. Another coaxial wire consisting of a sub-100 nm Au shell is presented in Figure S21. The position of elements with respect to each other confirms the coaxial nature of the deposition methodology.

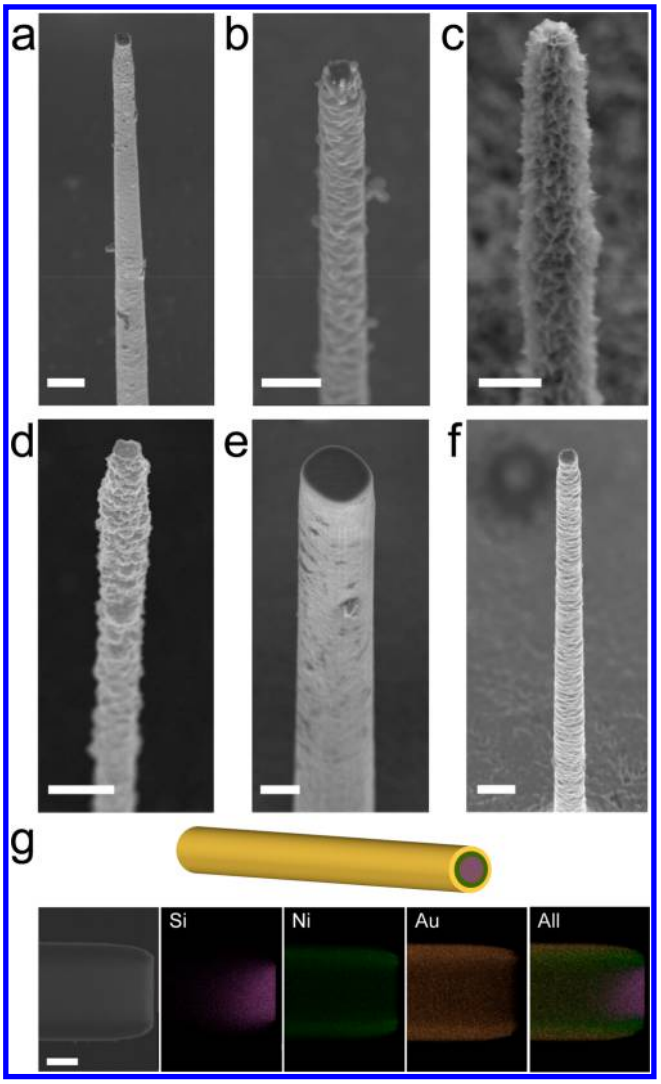

Figure 4. Materials library. Electron microscope images of different classes of materials demonstrated with (a) rhodium, (b) polyaniline, (c) manganese oxide, and (d) cadmium selenide covered wires. Hybrid and bimetallic layers are illustrated with SEM images of (e) Ni/polyaniline shell and (f) Ni/Ru shell. (g) Schematic, STEM image, and corresponding elemental maps of a Si−Ni−Au coaxial nanowire. Scale bar equals 1 μm for all images.

We have reported a facile electrodeposition method for the conformal deposition of functional layers onto high aspect ratio Si structures at fast rates and at room temperature with high fidelity. This method is applicable to various Si micro/nanowire structures and other material surfaces as long as the substrate is conductive and is particularly ideal for depositions of coaxial films. As the prevailing material in the electronics and photonics research and industry, modified Si structures prepared through this methodology hold promise to deliver complex architectures enabling novel applications in the fields of energy conversion and storage, sensing, and bioelectronics. Compatibility with organic materials, speed of deposition, and scalability of this method makes it a low-cost alternative and complementary approach to standard physical vapor deposition techniques.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.7b01950.

Detailed description of experimental methods and additional figures (PDF)

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T.O., B.A.Z., C.M.L., and D.G.N. designed the experiments. T.O., B.A.Z., R.G., and R.W.D. prepared the materials and collected the data. T.O., B.A.Z., R.G., R.W.D., C.M.L., and D.G.N. analyzed the data and wrote the manuscript.

Notes

The authors declare no competing financial interest.

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