10.1098/rsta.2004.1377

THE ROYAL SOCIETY

Semiconductor nanowire heterostructures

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Published online 8 April 2004

Recent progress on the synthesis and characterization of semiconductor nanowire heterostructures is reviewed. We describe a general method for heterostructure synthesis based on chemical vapour deposition and the vapour–liquid–solid growth of crystalline semiconducting nanowires. We then examine examples of nanowire heterostructures for which physical properties have been measured, considering the effects of synthetic conditions on the heterointerfaces as well as the electrical and optical characterization measurements that reveal heterointerface formation and quality. Finally, we identify areas of technical and conceptual progress that can contribute to the development of functional nanowire heterostructures.

Keywords: semiconductor; heterostructure; synthesis; nanowire; nanotechnology; chemical vapour deposition

1. Introduction

The motivation to manipulate matter on the nanometre scale arises not only from the fascinating emergence of novel behaviours at small length-scales, but also from the appeal of engineering material properties by building up from the nanoscale. A true nanotechnology based on materials built from the bottom up will require parallel and scalable means of fabrication. While several efforts in nanomaterials research may in time realize these goals, here we focus on semiconductor nanowires. For the purposes of this review, semiconductor nanowires are defined as free-standing semiconductor structures with diameters of a few to tens of nanometres with lengths of tens of nanometres to tens of microns formed by additive, synthetic means rather than subtractive methods such as lithography and etching. We will describe how useful heterojunctions can be built into semiconductor nanowires during synthesis, thereby providing complex, functional building blocks for nanotechnologies based on assembling materials from the bottom up.

Semiconductor electronic devices including field-effect transistors (FETs), bipolar transistors, modulation-doped high-mobility FETs, light emitting diodes (LEDs) and quantum cascade lasers have revolutionized science and technology since the invention of the transistor. The operating principles and performance of these devices

One contribution of 12 to a Discussion Meeting 'Organizing atoms: manipulation of matter on the sub-10 nm scale'.

are intimately related to functional interfaces and/or heterostructures within the devices (Sze 1981). These interfaces include dielectric–semiconductor junctions, semiconductor heterojunctions, p–n homojunctions and metal–semiconductor junctions. The functions performed by heterointerfaces include passivation, electrical isolation, charge transfer and internal field generation. Exquisite control over the composition and perfection of interfaces is required for the successful fabrication of high-performance planar devices, and is expected to be equally important in nanoscale devices given the inherently large surface area to volume ratios. The demonstration of lasing in core–shell semiconductor nanocrystals grown in solution provides an excellent example of the importance and utility of interface control in nanoscale materials (Nirmal & Brus 1999).

The impact of planar heterostructure technology has not been limited to commercial applications. The consequences for fundamental science include, for example, the ability to study electrons in reduced dimensions, enabling the discovery of the integer (Vonklitzing *et al*. 1980) and fractional (Tsui *et al*. 1982; Stormer *et al*. 1983) quantum Hall effects. Mesoscopic physics in general is enabled by two key technologies: atomically precise modulation of composition and doping perpendicular to planar thin films, and 10–100 nm scale control of semiconductor structures via lithography. New synthetic fabrication methods, some of which will be described here, enable the nanoscale control of additional device dimensions and provide prospects for uncovering new physics, new devices and new technology. The revolutionary impact of the aforementioned semiconductor heterostructures on fundamental science, as well as in daily life, provides ample motivation to pursue means of fabricating novel nanoheterostructures using parallel, scalable methods.

Here we review recent progress in the synthesis and characterization of semiconductor nanowire heterostructures. First, we review the synthesis of semiconductor nanowires using the vapour–liquid–solid growth mechanism. Second, we describe how control over axial and radial-growth modes provides a basis for novel nanowire heterostructures. Third, we examine examples of nanowire heterostructures for which physical properties have been measured, considering the synthetic techniques and conditions as well as those measurements that address the quality of the heterostructure thus formed. We discuss the technical issues most relevant to the functional heterostructure fabrication, identify measurements and insights needed to push the development of nanowire heterostructures forward, and suggest new types of devices enabled by the developments in synthesis.

2. Nanowire heterostructure synthesis

Semiconductor nanowires can be synthesized by employing metal nanoclusters to catalyse growth via a vapour–liquid–solid (VLS) process (figure 1) (Wagner 1970). Metal nanoclusters are heated above the eutectic temperature for the metal–semiconductor system of choice in the presence of a vapour-phase source of the semiconductor, e.g. silane (SiH_4) in the case of silicon. Adsorption of the vapour phase reactant on the metal catalyst leads to the formation of a liquid metal–semiconductor alloy (eutectic) at the surface that eventually consumes the entire catalyst particle. Continued adsorption of the semiconductor results in supersaturation of the liquid alloy, leading to nucleation of solid semiconductor and returning the system closer to

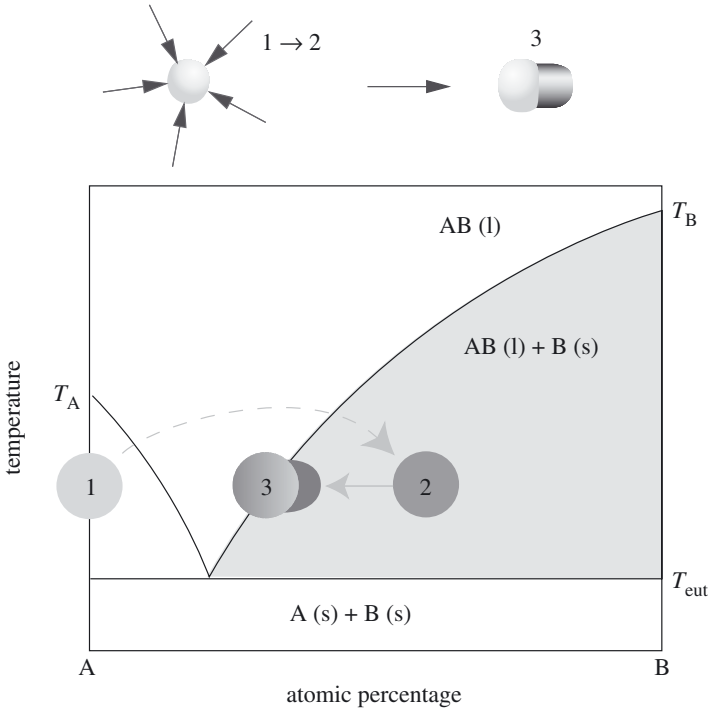

Figure 1. Binary phase diagram for metal (A) and semiconductor (B) illustrating the thermodynamics of vapour–liquid–solid growth. A source of B in the vapour phase causes the solid nanoparticle (1) to form a liquid eutectic AB. Continuous feeding of B produces supersaturation of the AB liquid particle (2), leading to nucleation of solid B (3).

an equilibrium in which the solid semiconductor surface is in contact with the metal–semiconductor liquid. The solid–liquid interface thus formed is the growth interface, as the semiconductor in solution condenses here to form the solid nanowire. Continuous vapour delivery provides the driving force for diffusion of the semiconductor from the liquid-catalyst particle surface to the growth interface.

Due to surface tension, the liquid catalyst forms a ball atop the growing nanowire. The diameter of nanowires grown by VLS is therefore determined by the diameter of the catalyst (Gudiksen & Lieber 2000; Cui *et al*. 2001). Preferred growth directions lie perpendicular to planes along which silicon atoms (in solution) diffuse readily, allowing for completion of said planes out to the diameter of the catalyst, presumably by incorporation of adatoms at step edges. At low temperatures, and with negligible vapour–solid growth on the nanowire surface, the extruded nanowire is nearly round, with a diameter matching that of the catalyst.

Once a nanowire has begun growing, there are actually two surfaces exposed to the vapour: that of the metal–semiconductor liquid and that of the solid semiconductor. To achieve one-dimensional axial growth, vapour adsorption should occur preferentially at the surface of the catalyst particle rather than on the surface of the semiconductor nanowire. In the case of silicon nanowires grown using silane (SiH_4), for example, we require that silane decomposition on the Au–Si surface be strongly preferred to decomposition on the presumably hydrogen-terminated nanowire surface. While silane will readily undergo dissociative chemisorption on a bare silicon

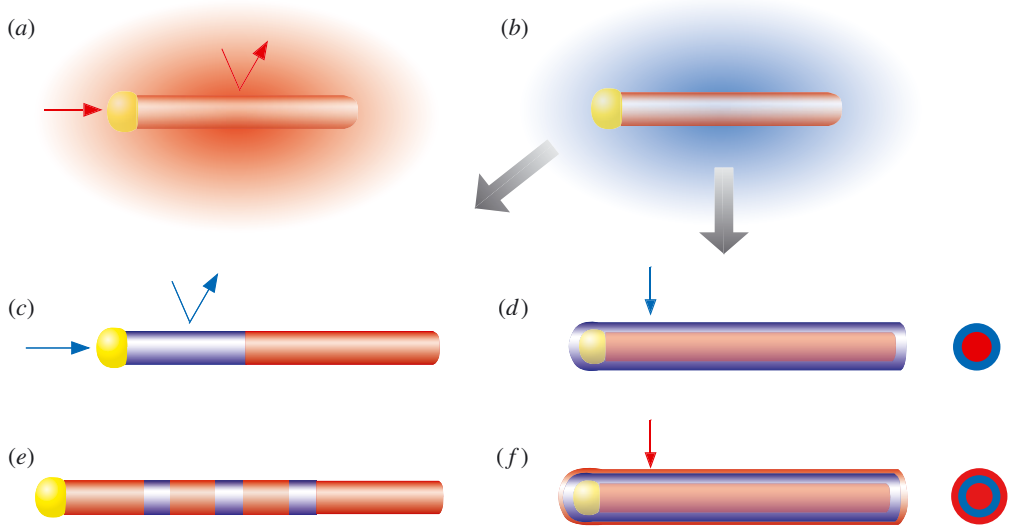

Figure 2. Nanowire heterostructure synthesis. (*a*) Preferential reactant incorporation at the catalyst (growth end) leads to one-dimensional axial growth. (*b*) A change in the reactant leads to either (*c*) axial heterostructure growth or (*d*) radial heterostructure growth depending on whether the reactant is preferentially incorporated (*c*) at the catalyst or (*d*) uniformly on the wire surface. Alternating reactants will produce (*e*) axial superlattices or (*f*) core-multi-shell structures.

surface, hydrogen termination may block adsorption sites at sufficiently low temperatures. In the absence of such a site-blocking mechanism, one would expect radial growth on the nanowire surface to occur simultaneously with one-dimensional axial growth. In the original experiments of Wagner, the whisker shape was attributed to a strong preference for Si atom incorporation at the liquid-catalyst rather than the solid-wire surface.

To understand the rational formation of nanowire heterostructures within the context of crystalline core growth by the VLS method, consider the possible effects of a change in reactant vapour once nanowire growth has been established (figure 2). If vapour decomposition/adsorption continues exclusively at the surface of the metal–semiconductor catalyst, crystalline growth of the new semiconductor will continue (figure 2*c*) and the width of the interface between the new and old semiconductors will be determined by depletion of the original semiconductor within the catalyst as well as by thermodynamic considerations. Details from actual experiments will be related below. On the other hand, if the new vapour/reactant does not decompose/adsorb exclusively at the catalyst surface, but also at the surface of the semiconductor nanowire, a shell of material will grow on the original nanowire surface (figure 2*d*). Control over the interfacial kinetics is therefore necessary to control the dominant growth mode. Radial shell growth is 'turned on' by adjusting reaction conditions to favour heterogeneous reactant decomposition. In general, the growth kinetics are controlled by varying the pressure, flow rate, temperature, reactant species and background gases that are byproducts of growth reactions.

The repeated changing of reactants in a regime favouring axial growth will lead to the formation of a nanowire superlattice, as shown in figure 2*e*. Similarly, chang-

ing reactants while in a radial-growth regime will result in core-multi-shell radial structures, as shown in figure 2*f*. Control over radial and axial growth allows for the production of complex heterostructures such as a zero-dimensional quantum dot within a one-dimensional nanowire capped by a shell of arbitrary composition. It is important to mention that there are few constraints on the composition of shell growth; any material suitable for planar film deposition can be deposited on the surface of a nanowire. Furthermore, the nanowire surface is crystalline, allowing for crystalline radial heteroepitaxy. For uniform coating, however, an isotropic reactant flux is required rather than a directed flux such as that produced by an effusive source.

3. Nanowire heterostructure properties

In this section, we review examples of nanowire heterostructures that have been synthesized by the VLS and catalyst-free methods, focusing primarily on those studies in which physical properties have been measured. For each study, we summarize the growth methods as well as those property measurements that related directly to the quality of the heterointerfaces within the wire. As described above, there are two basic structures to consider: axial heterostructures, in which the heterointerface is perpendicular to the wire axis, and radial heterostructures, in which the heterointerface is parallel to the wire axis. After reviewing the variety of structures made to date, we will be in a better position to identify developments necessary to further improve heterostructure quality and function.

(*a*) *Axial heterostructures*

Silicon whiskers with modulated doping concentration were made in the pioneering studies of Wagner (1970) for the purposes of elucidating the VLS growth mechanism. Electrical properties for these or other whisker structures were not reported at that time. While suggestions that the whiskers might behave as 'quantum wires' date back to at least the 1970s, the lithographic tools that enable such measurements were not widely available until recently. The essential anisotropy necessary for whisker growth, namely the favoured adsorption of silicon at the liquid-catalyst surface rather than the solid-wire surface, was recognized. In fact, radial homoepitaxial overgrowth was suggested as a means of growing large single crystals from small whiskers without the need for a substrate, or seed. Attempts to control or minimize radial overgrowth for the purposes of growing a more nearly one-dimensional whisker were not reported.

Haraguchi *et al*. (1992) made substantial progress on the growth of GaAs whiskers in the early 1990s, including the fabrication of p–n junctions within whiskers. They employed gold catalyst particles in a reduced-pressure (*ca*. 150 Torr, 400–600 °C) metal-organic chemical vapour deposition (MOCVD) reactor with trimethylgallium and arsine (AsH_3) as precursors to produce tapered nanowires of micron lengths and *ca*. 100 nm average diameters. Polarized electroluminescence was observed from large arrays of vertically aligned nanowires. The whiskers were determined to be the source of light emission, although the location of the emission within the wire was not determined. A blue-shift was observed relative to bulk p–n junctions and attributed to quantum confinement effects, but the simultaneous measurement of large numbers of nanowires of varying diameters precluded a definitive verification

of this claim. This issue was explored more fully in a later publication in which the authors also addressed the very important issue of surface passivation and surface depletion.

A significant step in the controlled synthesis of nanowire heterostructure was demonstrated by three groups with the growth of nanowire superlattices in a number of systems (Wu *et al*. 2002; Gudiksen *et al*. 2002; Bjork *et al*. 2002*b*). The Yang group combined thermal chemical vapour deposition using silane tetrachloride ($SiCl_4$) with the laser ablation of a solid germanium target to produce Si–SiGe nanowires (Wu *et al*. 2002). Wire growth was at 850–950 °C and 1 atm total pressure, with a $SiCl_4/H_2$ mole ratio of 0.02. The growth method did not result in substantial overcoating of the laser-ablated Ge; while this could indicate a higher sticking coefficient for Ge on the Au–Ge alloy liquid than on the semiconductor surface, it is also possible that background gases play a role. Though quantitative composition profiles were not reported, the interfaces were rather broad, and no property measurements were reported. One goal of the Si–SiGe superlattice synthesis was to make novel one-dimensional materials engineered to have a high thermoelectric coefficient. In a subsequent study, the same group measured the thermal conductivity of single Si–SiGe superlattice nanowires and concluded that phonon scattering was dominated by alloy scattering rather than Si–SiGe interface scattering (Li *et al*. 2003). Nonetheless, this remains a very promising research direction. Given the broad interfaces seen in other laser-ablation-grown superlattices (below), a strictly CVD-based approach would be desirable in the Si–Ge system.

Gudiksen *et al*. (2002) synthesized nanowire GaP–GaAs superlattices via alternating laser ablation of solid GaP and GaAs targets at temperatures of 700–850 °C at 100 Torr in a continuous argon flow. Pauses of 45 s were introduced between target switching. The lengths of the segments were controlled by the number of pulses delivered to each target. Photoluminescence microscopy revealed strongly emitting segments of the direct-gap GaAs alternating with 'dark' segments of the indirect-gap GaP, producing a unique sequence of 'on' and 'off' states that constituted an optical 'nanobarcode'. The interface widths in the GaP–GaAs superlattices were determined to be of the order of the catalyst particle size (*ca.* 20 nm) by energy-dispersive X-ray analysis in a scanning transmission electron microscope (TEM). This width is not surprising given the picture of VLS growth developed above; one might expect a gradual depletion of P and a gradual buildup of As via bulk diffusion through the catalyst following a change in target. The pause between target changes should serve to return the eutectic catalyst to equilibrium, but would not necessarily lead to depletion of the group V species, despite their relatively high volatilities compared with the group III constituents. The composition of the AuGaP and AuGaAs eutectics in this ternary system is not known however, and, furthermore, the potential role of surface transport has not been examined, as discussed further below.

Bjork *et al*. (2002*a*, *b*) were able to produce InP–InAs superlattices with very abrupt interfaces using ultrahigh vacuum chemical beam epitaxy. Wire growth catalysed by Au particles was performed at 420 °C and *ca.* 3 Torr using trimethylindium (TMIn), tertiarybutylphosphine and tertiarybutylarsine precursors. To create heterojunctions, the TMIn source was turned off, the group V source turned on after a 5 s pause, and the TMIn turned on again after another 5 s. High-resolution TEM (HRTEM) images were consistent with interface widths of a few atomic layers, though elemental analysis was not performed. The authors attributed the monolayer sharp-

ness of the interfaces to the high vapour pressures of the group V source materials in combination with the low growth rate (*ca.* 1 ML s^{-1}).

Using the techniques described above, InP barrier segments of varying lengths were embedded in InAs wires *ca.* 40 nm in diameter. Variable temperature electrical measurements of these wires were modelled by assuming that thermionic emission over the InP barrier was the primary temperature-dependent barrier to electron flow. A barrier height of 0.57 eV was determined, in good agreement with an expected barrier height of 0.6 eV. Continuing along similar lines, the same group synthesized a resonant tunnel diode (RTD) structure consisting of an InAs quantum dot between two InP barriers, all of which were embedded in an InAs nanowire (Bjork *et al.* 2002*c*). The RTD showed evidence of both radial and axial confinement, emphasizing the one-dimensional nature of the InAs dot. The observation of sharp spectral features in the tunnelling spectra, corresponding to well-defined quantum levels, was enabled by the very abrupt interfaces between InP and InAs segments: estimates from HRTEM indicate a 1–3-layer transition region. By changing the RTD device dimensions and applying a gate electrode to the central dot, a nanowire single-electron transistor was formed (Thelander *et al.* 2003). Reproducible fabrication of both the RTD and the SET with the desired performance characteristics requires very precise control over barrier widths and the ability to form abrupt interfaces. Though the electrical measurements do not quantitatively assess the barrier or interface widths, they provide an impressive demonstration that it is possible to form effective confinement potentials using interfaces within nanowires.

While semiconductor heterojunctions are prevalent and useful, p–n homojunctions are the basis of planar silicon FET technology and many semiconductor devices. Intrawire p–n junction diodes were fabricated within individual silicon nanowires by Gudiksen *et al.* by direct addition of gas phase dopants during the growth process (Gudiksen *et al.* 2002). To switch dopants, the dopant flow was turned off and the reactor evacuated with silane flowing before switching on the alternate dopant. Typical growth conditions were a temperature of 450 °C, a pressure of 10 Torr and silane flow rates of 3 standard cm^3 min^{-1}. In two-terminal electrical measurements, rectifying behaviour was clearly linked to the formation of a nanoscale p–n junction within single nanowires. The abrupt transition in carrier type and accompanying built-in potential barrier was revealed by simultaneous conductivity and atomic force microscopy measurements. For p–n junctions in InP nanowires, optical imaging of single nanowire emission clearly showed emission from the p–n junction, as opposed to, for example, the metal–semiconductor junction at the contact. While the imaging resolution of the AFM and optical techniques are insufficient to determine the abruptness of the p–n junctions, the resolution was sufficient to demonstrate that the function of the nanowire devices did derive from interfaces built into the nanowires at the time of synthesis. Recently, intrawire p–n diodes have also been fabricated in GaN nanowires grown by MOCVD (Cheng *et al.* 2003). The diode characteristics of single nanowires were measured at various temperatures and found to be consistent with electron tunnelling through a voltage-dependent barrier.

Photoluminescence measurements provide, in principle, a more straightforward means to verify that nanoheterostructures have produced quantum confinement of charge carriers, though caution is needed when interpreting energy shifts as evidence of quantum confinement because there are other possible origins of blue shifts. Several photoluminescence measurements have been done in II–VI and III–V direct-

gap systems, including ZnSe–CdSe (Solanki *et al.* 2002), ZnO–ZnMgO (Park *et al.* 2003), InAs–GaAs (Panev *et al.* 2003) and InAs–InP (Poole *et al.* 2003). In the case of ZnSe–CdSe, photoluminescence measurements were not performed with sufficient spectral resolution to identify the nature of the observed emission (Solanki *et al.* 2002). Park *et al.* (2003) observed quantum confinement in ZnO–ZnMgO nanorod heterostructures grown using catalyst-free metal-organic vapour phase epitaxy at 400 °C. The authors state that rods of presumably uncontrolled diameter form as a result of preferential growth along the *c*-axis of ZnO, but the seeding or nucleation of the wires was not discussed. ZnO–ZnMgO interface widths of the order of 1 nm were measured using HRTEM, though no significant Mg diffusion was expected at the growth temperature, and no catalyst was used. The widths were attributed to the fact that the growth interface is not perfectly flat, but rather rounded at the edges of the nanowire. (This highlights one challenge in using TEM to analyse nanowire heterointerfaces: the effective sample thickness vanishes towards the edge of a nanowire, making quantitative assessment of the structure and composition of the last few layers difficult.) A clear blue-shift in the photoluminescence peak energy with decreasing ZnO well width was observed, demonstrating quantum confinement in the axial direction. Radial confinement was not relevant as the wire diameters averaged *ca.* 40 nm. It should be noted that the measurements were performed on large numbers of nanorods oriented vertically on a substrate; this orientation is suitable for determining axial quantum confinement, but less so for radial in that it would give only an averaged value.

Panev *et al.* (2003) observed sharp exciton emission from InAs quantum dots inside GaAs nanowire hosts grown using similar techniques to those used for InAs–InP superlattices by the Samuelson group. While the growth temperature (510 °C) and pressure (*ca.* 2 Torr) were comparable with those used for the InAs–InP growths, the growth interrupts between group III sources were in this case several minutes. Simultaneous axial and radial growth produced tapered nanowires that effectively encapsulated the InAs dot within a GaAs shell. It was suggested that this tapering might be reduced by reducing the V/III ratio. The authors point out one potential benefit of such a structure, namely the natural *in situ* surface passivation resulting in increased radiative recombination. The peak energies emitted by the InAs dots were substantially blue shifted from the bulk InAs indicating that substantial alloying with the GaAs wire had occurred. Accordingly, the effects of possible confinement potentials on the peak energy could not be determined.

Poole *et al.* (2003) grew InP–InAs–InP nanowires on InP substrates without the use of a catalyst. TMIn and precracked AsH_3 and PH_3 were used as precursors at 505 °C. This catalyst-free method of whisker growth is based on the preferential diffusion of In along {110} facets and incorporation on {111} planes. The InAs quantum well thickness was not measured, but estimated to be 0.6 nm based on known growth rates for planar films. The assumption that planar and wire growth rates are the same is questionable, however, if the wire surface acts as a source of atoms for tip growth. During photoluminescence excitation at low power densities, a single well-defined peak was observed at 921 meV. At higher powers, excited state peaks were observed at energy spacings consistent with the quantum confinement of excitons within the estimated well widths. TEM imaging was not performed to confirm the quantum well width or explore the interfacial abruptness, nor was modelling undertaken to

explain the excited state energies, but the experiment does represent an important demonstration of exciton confinement in a nanowire heterostructure.

A comparison of the excitation spectrum in optical experiments and charging energies in nanowire SET devices informs the design of an electrically driven single photon source in a doped nanowire heterostructure, as has been demonstrated in planar quantum dot structures (Yuan *et al*. 2002). Recent demonstrations of optical (Huang *et al*. 2001) and electrically injected (Duan *et al*. 2003) lasing in nanowires are consistent with reasonable minority carrier lifetimes, which, when combined with observation of confinement at abrupt interfaces, suggest that such a single photon source may be feasible. Observing sub-Poissonian statistics in photon emission from a single nanowire would be an encouraging step towards this goal.

Despite the rapid progress demonstrated in the studies described above, much remains to be understood about the nature of heterointerface formation during whisker growth. Of particular interest is the difference in interfacial abruptness observed between different growth methods. It was determined by Wagner that the catalyst–wire interface was planar, but another important issue is whether the abruptness of the planar interface is limited by the method of precursor delivery and growth conditions or by the material system in question. These considerations naturally break down into distinctions between the influences of reaction kinetics versus thermodynamics. We expect that an appropriate phase diagram is a necessary but not sufficient condition for abrupt axial heterostructure growth, due to the obvious influence of kinetics on the systems studied to date. Catalyst-free methods are simpler to analyse in principle, and show promise, but are not as generally applicable as VLS methods due to their reliance on, for example, anisotropy in the diffusion on various crystal surfaces for a given system.

One factor to consider that has not, to our knowledge, been discussed in the context of nanowire heterostructures is the relative efficacy of mass transport via surface versus bulk diffusion. The question has been raised in the context of metal-catalysed carbon nanotube growth, but is also interesting to consider in, for example, III–V nanowire growth. If the majority of the group V component is delivered to the growth interface by surface diffusion, rather than bulk diffusion through the eutectic, it could be much easier to accomplish source depletion before switching. This is one possible explanation for the sharp interfaces observed by the Samuelson group. Note that this is not inconsistent with the broadened interfaces observed by Gudiksen *et al*. in the GaAs–GaP superlattices described above, as the studies were performed at different temperatures with different group III metals and different sources. A description of VLS heterostructure growth that encompasses both studies is very desirable.

(*b*) *Radial core–shell heterostructures*

Numerous examples exist of the incidental formation of core–shell structures in nanowire growth, the most prevalent being an oxide shell that forms due to high oxygen or water partial pressures in the reactor or the native oxide that forms upon exposure to air. Much less work has been done towards the rational design and synthesis of functional radial heterostructures. Here we wish to focus primarily on those studies in which core–shell semiconductor nanowires were produced in a deliberate and controlled manner.

The there are many important reasons to focus synthesis efforts on controlled radial heterostructure formation. First of all, nanowires have a very large surface-to-volume ratio. In a 10 nm silicon nanowire, for example, there are approximately 30 surface atoms for every 1000 bulk atoms. Expressed in terms of a bulk concentration, this corresponds to 1.5×10^{22} cm^{-3}. It is clear from this comparison that the passivation of interface states will be critical to nanoscale device performance, as surface states can have a number of deleterious effects. These include

(i) band bending induced by surface charge that could cause complete depletion of the nanowire;

(ii) a high density of surface states will mitigate the effect of an externally applied potential;

(iii) surface states can act as sinks for minority carriers, degrading the performance of optoelectronic devices and other minority carrier devices such as bipolar transistors;

(iv) the potential fluctuations associated with trapped charge at an interface can reduce carrier mobility.

Many of these negative consequences can be avoided by passivating the nanowire surface at the time of synthesis, i.e. immediately following core definition.

There are several positive reasons for exploring the synthetic possibilities following growth of a crystalline nanowire core. Consideration of materials that might be grown coaxially on a nanowire core leads directly to a number of potential applications for core–shell structures. A dielectric shell could provide both interface state passivation and electrical isolation. Furthermore, the use of a high K dielectric would be beneficial in nanowire FET applications. A shell dielectric could be used to form a high-quality optical cavity around a small core nanowire acting as the gain medium. A dissimilar semiconductor shell, or radial heterostructure, could be used to generate internal fields perpendicular to the interface to provide confinement potentials for carriers in either the core or shell. By combining a radial heterojunction with a layer of dopant atoms (modulation doping), a two-dimensional cylindrical quantum well could be populated with high-mobility charge carriers. More novel material combinations involving, for example, ferroelectric oxides on nanowire cores, offer the opportunity to make non-volatile RAM or tunable transceivers. Many of these applications will require the development of new nanowire handling and device fabrication methods, but the possibilities can be defined by beginning with the synthesis.

Lauhon *et al*. (2002) demonstrated a general method for controlled radial heterostructure growth that can be applied to produce to a variety of core–shell materials. The CVD-based approach was outlined earlier in this review. In essence, radial shell growth is 'turned on' by altering the reaction variables of temperature, gas composition, and pressure to favour uniform vapour phase deposition on the nanowire surface. The controlled growth of a radial homoepitaxial shell was demonstrated for i-Si–p-Si core–shell wires, in which the introduction of diborane during silane-based nanowire growth led to substantial radial growth and the deposition of a p-Si shell. The partly crystalline p-Si shell could be fully crystallized by annealing. The field effect mobilities of i-Si–p-Si nanowires reflected the degree of crystallinity; amorphous, polycrystalline and crystalline p-Si shells exhibited successively increasing mobilities as expected.

Diborane is known to increase the growth rate of silicon films in planar CVD by producing more reactive precursors and complexes in the gas phase. In the context of nanowire growth, we believe that while the site-blocking effect of hydrogen-terminated silicon is sufficient to prevent the dissociative adsorption of silane under certain conditions, other species produced by the diborane are more reactive. The observation that a substantial background hydrogen partial pressure mitigates p-Si shell growth is consistent with this explanation. The effect of hydrogen on Ge nanowire growth also supports the role of hydrogen in minimizing shell growth, either by suppressing H desorption or by suppressing gas phase decomposition reactions (Wang *et al*. 2003; Greytak *et al*. 2004).

Lauhon *et al*. also synthesized Si–Ge and Ge–Si core–shell heterostructures, again by adjusting reaction conditions to move from a core growth to a shell growth regime. For the case of Si–Ge core–shell nanowires, switching the reactants from silane to germane, while maintaining typical silicon nanowire growth conditions, produced a change from Si core to Ge shell growth, presumably due to the more facile thermal decomposition of germane. The germane growth was epitaxial, suggesting a substantial surface mobility for Ge adatoms. Si shells grown on Ge nanowires, while not crystalline as deposited, could be crystallized by annealing. Interface widths for Si–Ge and Ge–Si core–shell wires were determined to be less than 1.5 nm. No measurable broadening of the interface Si–Ge interface was induced by the annealing process.

The electrical properties of Si–Si and Si–Ge nanowires reflected their non-uniform composition. Electrical transport measurements on p-Si–i-Ge and i-Ge–p-Si core–shell wires revealed evidence of charge transfer and confinement due to the valence band offset between silicon and germanium. While a quantitative determination of the offset was not made, the result does suggest the possibility of forming a radial modulation-doped FET with a similar structure to that of a planar MOD-FET. Towards this goal, a conducting p-Si–i-Ge core–shell wire was coated *in situ* with silicon oxide using oxygen and silane, and finally coated with a conducting layer of p-Ge. After suitable processing and device fabrication, these complex core–shell nanowires were used as the basis of a high-performance coaxially gated nanowire FET. This device demonstrated the possibility of making a modulation-doped radial core–shell FET with a one-dimensional channel or a cylindrical 2d carrier gas, but substantial synthesis and characterization work will be required to achieve this goal. Many of the challenges lie in adapting routine characterization methods to nanoscale devices. For example, though the gate coupling of these FETs can be larger than that of back-gated nanowire FETs, the capacitance is still sufficiently small to preclude conventional capacitance–voltage (C–V) measurements; C–V measurements are one means to perform electronic spectroscopy of interface states that provide valuable input to the device optimization process. Similarly, Hall measurements on macroscopic planar devices can be used to determine the majority and minority carrier concentrations, but such measurements cannot be easily or perhaps even meaningfully performed on a 10 nm nanowire. Many exciting challenges lie ahead in the pursuit of new tools and methods for nanostructure characterization.

Beyond the high mobilities associated with modulation-doped FETs, there are additional motivations for exploring alternatives to bulk doping in nanostructures. Even at moderate doping levels, very small nanowires will experience large fluctua-

tions in dopant density if they are 'bulk' doped for the simple reason that there are very few dopant atoms to begin with. A 10 nm nanowire doped at 10^{18} cm^{-3}, for example, has on average one dopant atom every 13 nm. The average dopant density fluctuation in a 60 nm long channel would be greater than 50%. Furthermore, as the surface-to-volume ratio increases, the effects of any dopant segregation during VLS growth will be amplified. Both of these considerations motivated the synthesis of surface-doped Ge nanowires for FET applications with the goal of remote doping in a self-limiting monolayer (Greytak *et al*. 2004); under certain conditions, the adsorption of dopant atoms can be self-limiting, suggesting a route to the controlled doping of nanostructures that can minimize potential fluctuations. We have recently fabricated complementary germanium nanowire FETs based on *in situ* surface doping with phosphine or diborane. Surface dopants were active and effective in determining the majority carrier type in 10 nm wires, though it was not possible to quantitatively determine the amount of dopant deposited.

The focus on electronic properties in Si–Ge nanowires in the studies of Lauhon *et al*. was due to the indirect band gaps of Si and Ge. Goldberger *et al*. (2003) recently demonstrated the formation of GaN–AlGaN nitride radial heterostructures, which, though formed spontaneously, might be very useful in optical applications. The lasing thresholds, for example, in both optically pumped and electrically injected nanowire lasers could be reduced through proper choice of a dielectric (insulating or wide bandgap) shell. The authors additionally noted that tube-like structures could be formed by preferential etching. Guidance on improving and engineering the optical properties in core–shell nanowires can be taken from the more advanced work done on core–shell nanocrystal systems.

4. Future directions

The benefits of functional heterostructures in nanowire devices have been discussed primarily in terms of improved single-wire device performance. In addition, the synthetic techniques described above are expected to be enabling with respect to the *assembly* of nanowires into more complex superstructures. Axial heterostructures of modulated doping and composition, for example, can form the basis of a stochastic decoder array (DeHon *et al*. 2003). Oxide overcoating on semiconducting nanowires may be used to determine the pitch of nanowire arrays self-assembled at fluid interfaces (Whang *et al*. 2003). One important motivation for basing a bottom-up technology on chemical methods of synthesis and assembly is that the fabrication methods are inherently parallel and often scalable. By building in functionality to nanoscale building blocks at the time of synthesis, we create new means to confront the challenge of parallel assembly. Conversely, there are many opportunities for the proposed methods of assembly to constructively inform nanowire heterostructure synthesis.

The original research described in this article was performed one while one of us (L.J.L.) was a postdoctoral researcher in the laboratory of Professor Charles M. Lieber in the Department of Chemistry and Chemical Biology, Harvard University. Other co-workers in the efforts mentioned above included Yi Cui, David Smith, Jianfang Wang and Deli Wang. M.S.G. thanks the National Science Foundation for predoctoral fellowship support. C.M.L. acknowledges the support of the Office of Naval Research and the Defense Advanced Research Projects Agency.

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