Supporting Information

Fu et al. 10.1073/pnas.1323389111

SI Text

Silicon Nanowire Synthesis. Boron-doped p-type silicon nanowires (SiNWs) were synthesized using a gold (Au) nanoparticle-catalyzed chemical vapor deposition (CVD) methodology described previously (1). In brief, 100-nm-diameter Au nanoparticles (Ted Pella, Inc.) were dispersed on an oxidized silicon (Si) wafer [600 nm silicon dioxide (SiO_2); Nova Electronic Materials]. Syntheses were carried out at 450–460 °C and 25 torr, with 2.5 standard cubic centimeters per minute (sccm) pure silane (SiH_4) as the silicon source, 3 sccm diborane (B_2H_6) (100 ppm in He) as the boron (B) dopant source and 10 sccm argon (Ar) as the carrier gas. Under these conditions, the resulting SiNWs have diameters of ca.100 nm and a delivered doping ratio of 4000:1 (Si:B). The total growth time was 40 min.

SiNW Field-Effect Transistor (FET) Fabrication. SiNWs were suspended in isopropanol solution by gentle sonication (2–3 s, 30 W; Crest Ultrasonics) and then dispersed onto the silicon nitride (Si_3N_4) surface of a Si wafer (100-nm thermal SiO_2, 200-nm Si_3N_4, n-type, 0.005 V · cm; Nova Electronic Materials) with predefined outer electrodes (Ti/Pt/Ti, 5/50/30 nm) and markers (Ti/Pt, 5/50 nm). The dispersed SiNWs were spin coated (4,000 rpm for 40 s, each layer) with resists [MMA (8.5), MAA (EL9) and PMMA (950, C2); MicroChem Corp.], and each layer was baked at 185 °C for 5 min. Electron-beam-lithography (EBL; JEOL-7000F) was used to define source/drain (S/D) contacts on individual SiNWs. The typical width of the contacts was 400 nm and the separation between S/D was 600–800 nm. A step of BHF (Buffered HF Improved, Transene) was carried out to eliminate natural SiO_2 on SiNW before thermal evaporation (Sharon Thermal Evaporator) of Ti contact (140 nm thick). A schematic of SiNW FET fabrication is presented in Fig. S1 *A* and *B*.

Germanium Nanowire Synthesis. Germanium nanowires (GeNWs) were grown on top of the resulting SiNW FETs as follows: First, 35-nm-thick Au nanodots with ca. 80-nm diameter were defined by EBL and thermal evaporation on top of SiNW FETs between predefined S/D (Fig. S1*C*). Second, the chip was placed in the CVD reactor, and GeNW growth was initiated by nucleation at 315 °C, and 300 torr for 1 min with 20 sccm germane (GeH_4) [10% in hydrogen (H_2)] as the germanium source, 200 sccm H_2 as the carrier gas, followed by elongation step at 285 °C, and 100 torr for 20–40 min (gas flow same as for nucleation). The resulting GeNWs have lengths ca. 3–4 μm and a slight taper with bottom diameters ca. 80–90 nm and top diameters ca. 50–60 nm (Fig. S1*D*).

GeNW Diameter Reduction. The upper 80% portion of the GeNWs were etched in hydrogen peroxide (H_2O_2) solution to reduce their diameters: (*i*) A diluted photoresist protection layer (Shipley S1805: Thinner Type P = 1:1; MicroChem Corp) with a thickness of ca. 20% of GeNW length was spin coated to cover the bottom part of GeNWs (Fig. S1*E*) and baked at 115 °C for 5 min. (*ii*) The chip was then placed in 0.17% H_2O_2 solution at 0 °C, and etched for 2–2.5 min; the calibrated H_2O_2 etching rate was 10–12 nm/min. (*iii*) After etching, the photoresist layer was removed in acetone (without drying), subsequently transferred to 200-proof ethanol, and dried with critical point dryer (Auto Samdri 815 Series A; Tousimis). The resulting GeNWs had 5–10-nm diameters (controlled by etching time) for the upper 80% portion and 80–90-nm diameters for the lower 20% portion of the GeNWs (Fig. S1*F*).

Nanotube Fabrication. To fabricate thin but mechanically robust SiO_2 nanotubes, we combined atomic layer deposition (ALD) and a two-step BHF etching as follows: First, a uniform 30 nm SiO_2 layer, which serves as both the nanotube wall and metal electrode passivation, was conformally deposited by ALD (Savannah-S200; Cambridge NanoTech) at 250 °C (Fig. S1*G*). Second, a photoresist protection layer (~20% of GeNW length) was spin coated and baked (Fig. S1*H*), and then the upper unprotected part of the SiO_2 layer was etched in BHF (Buffered HF Improved; Transene) to ~10 nm (Fig. S1, *I*); the etching rate was ~1.5 nm/min and was calibrated. Third, following liftoff of the former protection resist layer, a thicker photoresist layer (Shipley S1813 or S1818; MicroChem Corp.) was spin coated and baked at 115 °C for 5 min as shown in Fig. S1*J*. A second step of BHF etching was used to remove the exposed SiO_2 layer at the GeNW tip; the SiO_2 shell is tapered during this step due to etching along the axial and radial direction (Fig. S1*K*). After photoresist liftoff, the chip was transferred to H_2O_2 solution (30%; Sigma) to etch selectively the Ge (60 °C, 60 min), which produces the nanotube probe, and then the chip was dried in the critical point dryer. The resulting nanotubes have an inner diameter 5–10 nm and 10 nm tapered SiO_2 wall for the upper 80% portion and an inner diameter 80–90-nm and 30-nm SiO_2 wall for the lower 20% part (Fig. S1*L*).

Device Electrical Characterization. The behavior of the ultrasmall BIT-FET devices in aqueous solution was characterized in two distinct ways to determine their quasi-static and dynamic responses. (*i*) Standard quasi-static water-gate measurements were carried out in 1x phosphate buffered saline (1x PBS; Mediatech, Inc.) to characterize the device sensitivity as follows: The water-gate potential, V_{wg}, was varied at 50 mV/s (via Ag/AgCl electrode) while monitoring the SiNW FET current for fixed 100-mV S/D voltage; the FET current was amplified (1211; DL Instruments) and digitized at 100-kHz sampling rate (Axon Digidata 1440A Data Acquisition System; Molecular Devices, Inc.). The resulting current versus V_{wg} curves are used to calibrate the sensitivity (transconductance) for the devices. (*ii*) A quasi-step-function water-gate pulse was used to characterize the bandwidth (BW) of the ultrasmall BIT-FET devices in different concentration PBS solutions. In short, a 0.01 ms rise-time 100-mV amplitude V_{wg} step was applied (Axon Digidata 1440A Data Acquisition System; Molecular Devices, Inc.) while simultaneously recording the corresponding current variation of the ultrasmall BIT-FET, which was amplified, filtered at 30 kHz (CyberAmp 380; Molecular Devices, Inc.), and then digitized at a 100-kHz sampling rate. A 100-mV DC source voltage was used in all of the measurements.

Device Bandwidth Model. The calculation of the ultrasmall BIT-FET bandwidth is based on the model described for conventional BIT-FETs in ref. 1, and the equivalent circuit is shown in Fig. S5. With an applied step water-gate pulse [i.e., $V_{out} = V_0\theta(t)$ with V_0 being the pulse amplitude and $\theta(t)$ is the step function equals 1 for $t > 0$ and 0 for $t < 0$], this circuit can be described by the following partial differential equation,

$$\frac{\partial^2 V_{in}}{\partial z^2} = \rho_R \rho_C \left(\frac{\partial V_{in}}{\partial t} - \frac{\partial V_{out}}{\partial t} \right) = \rho_R \rho_C \left(\frac{\partial V_{in}}{\partial t} - V_0 \delta(t) \right), \qquad [S1]$$

where V_{in}, V_{out}, ρ_R, ρ_C, z, and t correspond to the potential inside the ultrasmall nanotube, the potential outside the nanotube, the linear resistivity of the solution inside the tube, the capacitance

of the ultrasmall nanotube wall per unit length, the distance from the nanotube opening, and time, respectively.

For numerical simulations (models 1 and 2 in Fig. 2*D*), we used a 1D finite-element method to evaluate the potential change at the end of the SiO_2 nanotube as a function of time following Eq. **S1**. We fixed the length of SiO_2 nanotube $L = 2.5$ μm and the thickness as $d = 10$ nm. Two models corresponding to the upper and lower bandwidth limits were considered. In model 1, the active channel is limited to the area defined by the GeNW base, and in model 2, the active channel corresponds to the entire active SiNW surface. These two models represented the scenarios of no Ge overcoating and complete Ge overcoating (we use a 10-nm Ge overcoating thickness based on experimental data; this Ge is removed during GeNW etching to produce the larger active area), respectively, on the SiNW.

Previous simulation results (1) revealed that the device bandwidth is mainly limited by the small diameter nanotube, and thus, that the tip access impedance and capacitive coupling to underlying SiNW FET can be ignored. We used these simplifications and the initial condition of $V_{in}(z,0) = 0$, we used the Laplace transform to obtain an analytical solution for Eq. **S1** as,

$$\frac{V_{in}}{V_0} = \frac{1}{\sqrt{\pi}} \int_0^{\frac{4t}{\rho_R \rho_c z^2}} \frac{\exp\left(-\frac{1}{x}\right)}{x^{\frac{3}{2}}}\, dx. \qquad \textbf{[S2]}$$

Because bandwidth is inversely proportional to the time needed for $\frac{V_{in}}{V_0}$ to increase from 0.1 to 0.9, we obtain

$$BW \propto \frac{1}{t_{0.9} - t_{0.1}} \propto \frac{1}{\rho_R \rho_C L^2} \propto \frac{\ln\left(1 + \frac{2t_{SiO_2}}{d}\right) d^2}{\rho_{sol}\ L^2}, \qquad \textbf{[S3]}$$

where ρ_R, ρ_C, d, t_{SiO_2}, L, and ρ_{sol} are the solution linear resistivity, effective nanotube wall capacitance per unit length, nanotube inner diameter, nanotube thickness, nanotube length, and liquid resistivity, respectively. Based on this relation, we can rescale measured bandwidth results by nanotube diameter, length, or liquid resistivity (conductivity).

Effect of Phospholipid Modification on Device Bandwidth. From Eq. **S3**, we can estimate the effect of phospholipid modification on device bandwidth by considering the change of ρ_R and ρ_C. For example, if phospholipid bilayers modify both inner and outer surfaces of the tube, ρ_R increases to $\left(\frac{d}{d-2t_{lipid}}\right)^2 \rho_R$ resulting from the reduction of the effective nanotube inner diameter and ρ_C decreases to $\frac{\rho_C}{1 + \frac{\varepsilon_{rSiO_2}}{\varepsilon_{rlipid}} \frac{\ln\left(\frac{d}{d-2t_{lipid}}\right) + \ln\left[\frac{d+2(t_{SiO_2}+t_{lipid})}{d+2t_{SiO_2}}\right]}{\ln\left(\frac{d+2t_{SiO_2}}{d}\right)}}$ because the lipid bilayers act as new capacitors connected with the nanotube wall capacitor in series. Here, t_{lipid}, ε_{rSiO_2}, and ε_{rlipid} are double-layer phospholipid thickness (ca. 4.75 nm; ref. 2), relative dielectric constant of SiO_2 (ca. 3.9; ref. 3) and relative dielectric constant of bilayer phospholipid (ca. 5; ref. 4). From Eq. **S3**, the ratio of the bandwidth after to before modification can be expressed as:

$$\frac{BW_{after}}{BW_{before}} = \frac{(d - 2t_{lipid})^2}{d^2} \times \left\{1 + \frac{\varepsilon_{rSiO_2}}{\varepsilon_{rlipid}} \frac{\ln\left(\frac{d}{d-2t_{lipid}}\right) + \ln\left[\frac{d+2(t_{SiO_2}+t_{lipid})}{d+2t_{SiO_2}}\right]}{\ln\left(\frac{d+2t_{SiO_2}}{d}\right)}\right\}. \qquad \textbf{[S4]}$$

This ratio versus nanotube inner diameter is plotted in Fig. 4*C* (100%, red line) of the main text. Similarly, we obtain expressions for bandwidth ratio for the cases where the inner surface is only half covered and not covered at all. The nanotube inner-diameter dependence of these ratios is plotted in Fig. 4*C* (50%, green line and 0%, blue line).

1. Duan X, et al. (2012) Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor. *Nat Nanotechnol* 7(3):174–179.
2. Stern HA, Feller SE (2003) Calculation of the dielectric permittivity profile for a nonuniform system: Application to a lipid bilayer simulation. *J Chem Phys* 118(7): 3401–3412.
3. Gray PR (2009) *Analysis and design of analog integrated circuits* (Wiley, New York), 5th Ed.
4. Weaver JC, Schoenbach KH (2003) Biodielectrics. *IEEE Trans Dielectr Electr Insul* 10(5): 715–716.

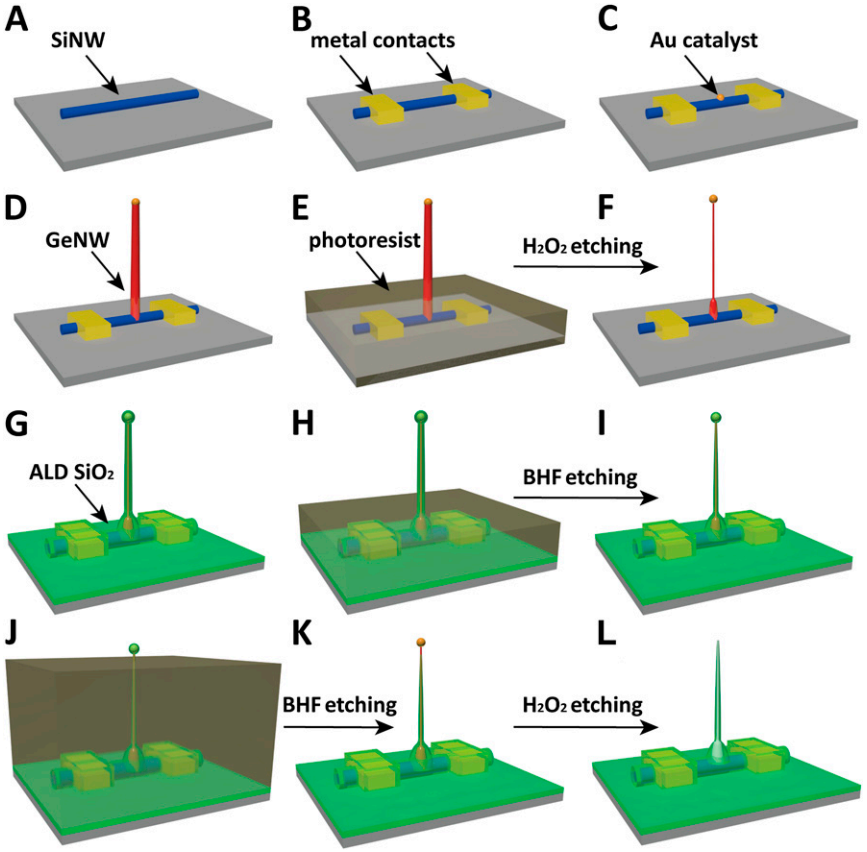

Fig. S1. Schematics of the fabrication flow for the ultrasmall BIT-FET. (*A*) SiNWs (blue) are dispersed on substrate (solid gray). (*B*) S/D contacts are defined by EBL followed by thermal evaporation. (*C*) Au nanodots are defined on SiNWs between S/D using EBL and thermal evaporation. (*D*) GeNWs (red) are grown on top of the SiNWs through nanocluster-catalyzed CVD process. (*E*) A thin layer of photoresist (transparent gray) is spin coated on the chip to protect the lower GeNW part. (*F*) The resulting H_2O_2-etched GeNWs following photoresist liftoff. Only the GeNW above the photoresist in *E* is thinned by etching in H_2O_2. (*G*) SiO_2 is conformally deposited over the entire chip by ALD. (*H*) A thin layer of photoresist (transparent gray) is spin coated to protect the lower region of chip. (*I*) The resulting BHF etched structures following liftoff. The region of SiO_2 above the photoresist layer in *H* is etched to ca.10-nm thickness. (*J*) Photoresist with thickness smaller than the GeNW heights is deposited. (*K*) The resulting structure following BHF etching of SiO_2, which exposes the tips of the GeNWs. Isotopic BHF etching yields a small taper with thinner SiO_2 at the topmost part of the structure. (*L*) The GeNW is removed by H_2O_2 etching to form an ultrasmall nanotube connected to the bottom SiNW FET.

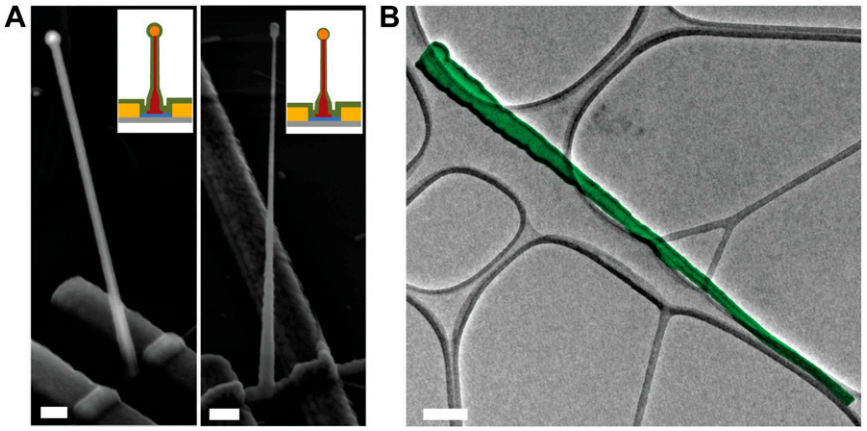

Fig. S2. Electron microscopy characterization of the ultrasmall BIT-FET. (*A*) Representative SEM (Zeiss Ultra Plus field-emission SEM) images of intermediate fabrication steps of the ultrasmall BIT-FET. (*Left*) Device after 30-nm ALD coating of SiO_2. (*Right*) Device after first step of selective BHF etching of the upper 80% portion of the SiO_2 to ca. 10 nm (Fig. S1 *H* and *I*). White dashed lines in *I* and *II* indicate the point below which the SiO_2 is protected by photoresist during BHF etching. Scale bars: 200 nm. (*B*) False-colored transmission electron microscopy (JEOL 2100 TEM) image of an ultrasmall nanotube. This tube was fabricated following the same procedure as described in *SI Text*, and deposited onto lacey carbon grids (Ted Pella) from ethanol suspension. It has a tip ID ~7 nm and bottom ID ~80 nm. False color is used here to distinguish the SiO_2 nanotube from background amorphous carbon. Scale bar: 50 nm.

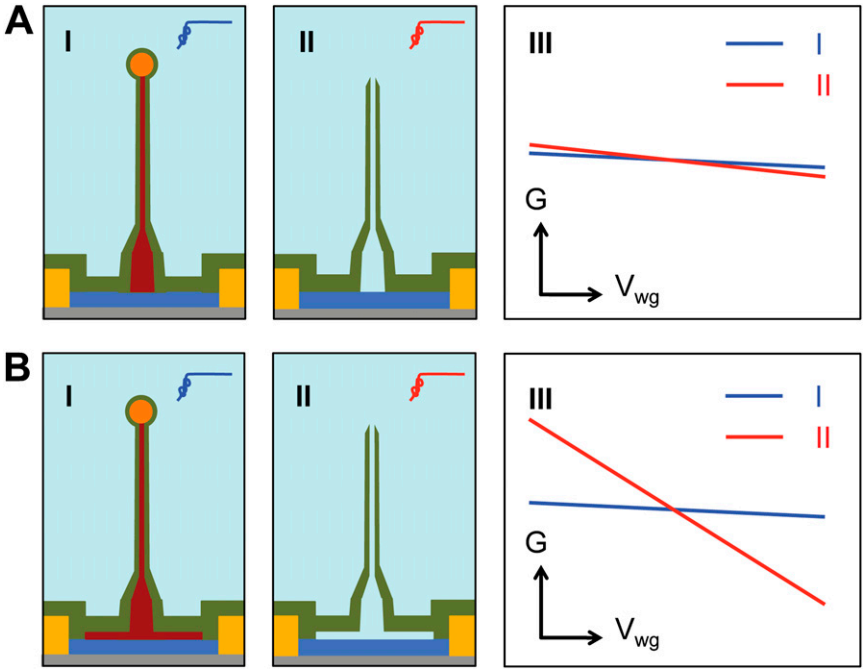

Fig. S3. Sensitivity of different device structures. (*A*, *B*) Schematics of the ultrasmall BIT-FET without and with Ge overcoating on the SiNW, respectively. *I* and *II* correspond to the BIT-FET devices before and after Ge core etching. *III* show schematically typical conductance (*G*) vs. water-gate (V_{wg}) measurements from these distinct structures.

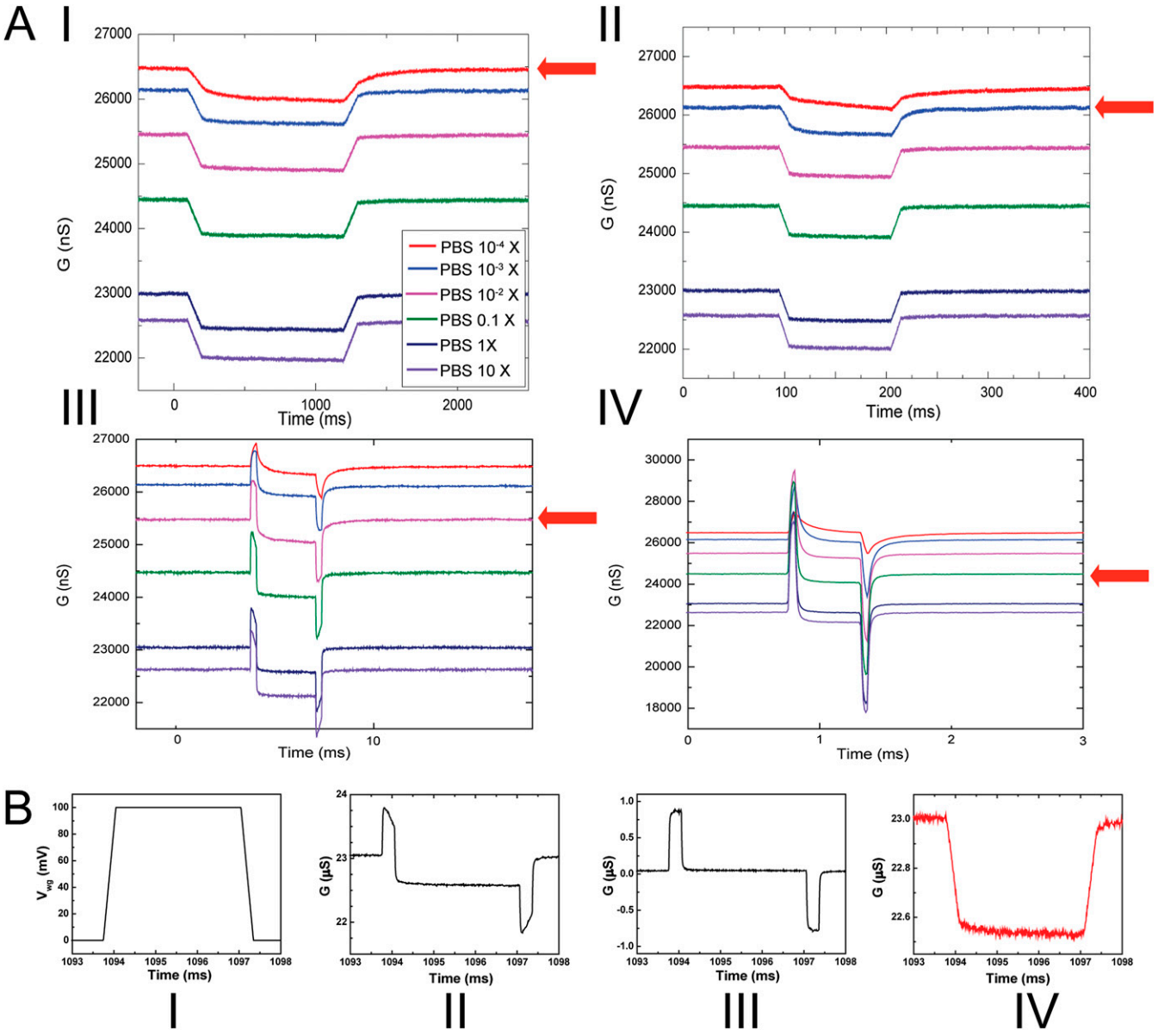

Fig. S4. Dynamic water-gate responses from ultrasmall BIT-FETs. (*A*) Pulsed (i.e., step function) V_{wg} and corresponding conductance (*G*) vs. time responses from a 10-nm ID ultrasmall BIT-FET in different concentration PBS solutions. The applied V_{wg} with a 100-mV amplitude pulses had rise/fall times of (*I*) 100, (*II*) 10, (*III*) 0.3, and (*IV*) 0.05 ms. The duration of the pulse is 10 times the rise/fall time in all measurements. The peak and dip features associating with the rise and fall of the water-gate pulse are due to the capacitive coupling to passivated metal electrodes (Fig. S1). Red arrows indicate the PBS solution concentration at which the ultrasmall BIT-FET response can no longer respond to the applied water-gate pulse without time delay. (*B*) Removal of capacitive signals from the passivated metal electrodes. A 100-mV pulsed water-gate V_{wg} with 0.3-ms rise/fall time was applied (*I*). Experimental responses from both ultrasmall BIT-FET and passivated metal electrodes (*II*), and only the passivated metal electrodes [i.e., V(S/D) = 0] (*III*) are shown. Subtraction of (*III*) from (*II*) yields the pure field-effect response from the ultrasmall BIT-FET (*IV*).

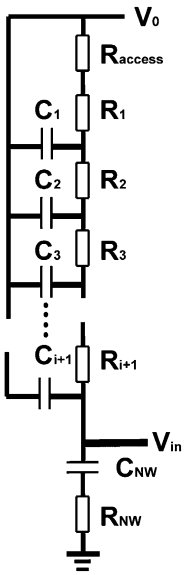

Fig. S5. Device bandwidth circuit model. Equivalent circuit used for the BIT-FET device bandwidth model.