# Vertically integrated, three-dimensional nanowire complementary metal-oxide-semiconductor circuits

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**Three-dimensional (3D), multi-transistor-layer, integrated circuits represent an important technological pursuit promising advantages in integration density, operation speed, and power consumption compared with 2D circuits. We report fully functional, 3D integrated complementary metal-oxide-semiconductor (CMOS) circuits based on separate interconnected layers of high-mobility n-type indium arsenide (n-InAs) and p-type germanium/silicon core/shell (p-Ge/Si) nanowire (NW) field-effect transistors (FETs). The DC voltage output ($V_{out}$) versus input ($V_{in}$) response of vertically interconnected CMOS inverters showed sharp switching at close to the ideal value of one-half the supply voltage and, moreover, exhibited substantial DC gain of ≈45. The gain and the rail-to-rail output switching are consistent with the large noise margin and minimal static power consumption of CMOS. Vertically interconnected, three-stage CMOS ring oscillators were also fabricated by using layer-1 InAs NW n-FETs and layer-2 Ge/Si NW p-FETs. Significantly, measurements of these circuits demonstrated stable, self-sustained oscillations with a maximum frequency of 108 MHz, which represents the highest-frequency integrated circuit based on chemically synthesized nanoscale materials. These results highlight the flexibility of bottom-up assembly of distinct nanoscale materials and suggest substantial promise for 3D integrated circuits.**

3D | integrated circuits | multilayer assembly | nanoelectronics

Integration of transistors into a single layer is currently the dominant implementation of integrated circuits in electronics. Three-dimensional integrated circuits consisting of multiple transistor layers can, however, offer significant performance advantages, including larger integration density, faster operation speed, and lower power consumption. These benefits have motivated substantial research in the electronics community to realize 3D integrated circuits (1, 2). While these efforts have been based mainly on conventional top-down approaches (1, 2), chemically synthesized semiconductor nanowires (NWs) (3–5) and carbon nanotubes (CNTs) (6–8) offer an attractive alternative approach to construct 3D integrated circuits. Specifically, these nanoscale building blocks can be assembled layer-by-layer into 3D structures, where sequential layers can readily be formed with the same or distinct nanomaterials (9, 10), a capability that is difficult to achieve by conventional top-down approaches (11). In the case of NWs, facile combination of distinct nanoscale materials (12, 13) with widely tunable nanoscale compositions and structures (14, 15) might enable 3D integrated circuits with unique capabilities.

To date, two reports (9, 10) have investigated 3D integration of nanoscale materials. This work has shown that sequential printing of NWs, nanoribbons, and/or CNTs is a viable approach for constructing 3D integrated circuits on conventional and plastic substrates. In addition, complementary metal-oxide-semiconductor (CMOS) configuration was also attained (9). Although these reports represent key steps toward 3D integrated NW and CNT circuits, they fall short of demonstrating features central to CMOS integrated circuits, including (*i*) control of switching thresholds, (*ii*) realization of full-swing operation for CMOS devices, and (*iii*) AC operation at high speed. In this work, we address these central issues through the fabrication and demonstration of functional 3D integrated NW CMOS inverter logic gates and high-frequency ring oscillators.

We use layer-by-layer assembly of indium arsenide (InAs) NW n-type field-effect transistors (n-FETs) (16–18) and germanium/silicon (Ge/Si) core/shell NW p-type FETs (p-FETs) (14, 19, 20) to fabricate vertically interconnected, 3D CMOS inverters and ring oscillators. The choice of a group-III/V material and group-IV heterostructure was motivated by the high-performance demonstrated previously for the corresponding NW FETs (18, 20), the desire to determine whether such distinct materials systems could indeed yield functional circuits through a bottom-up approach, and the corresponding current interest in hetero-integration of these two systems by conventional top-down fabrication to extend scaling in microelectronics (21).

## Results and Discussion

We explored our approach first for vertically interconnected, 3D CMOS inverter logic gates, where InAs NW n-FETs and Ge/Si NW p-FETs were used in the first and second layers, respectively (Fig. 1*A*). Key steps in the fabrication are as follows (see *Materials and Methods*). First, the lower layer of InAs NW n-FETs are fabricated by sequential steps of NW contact printing, source/drain (S/D) deposition, atomic layer deposition (ALD) of high-$\kappa$ dielectric, and top-gate (G) deposition. Second, a low-$\kappa$ dielectric was deposited to electrically isolate the initial NW FET layer, and then the same steps of NW deposition and fabrication were repeated to define the second layer of NW FETs. p-Ge/Si NWs were used in the second layer. Third, interconnections between NW n-FETs in layer-1 and NW p-FETs in layer-2 were made by combining via dry-etching and metal deposition (see *Materials and Methods*), in order to form a CMOS inverter.

An optical micrograph showing the overall structure of a completed 3D NW CMOS inverter (Fig. 1*B*) shows (*i*) light-blue first-level and brown second-level NW FET S/D electrodes and (*ii*) the well-defined interconnections at gate and drain electrodes of FETs in the two layers. A schematic structure of the vertical interconnection between the layer-1 and layer-2 gate electrodes (Fig. 1*C*) highlights our surface contact strategy for making the vertical interconnection of the non-overlapping gates in the two layers (see *Materials and Methods*). A scanning electron microscopy (SEM) image of the interconnect region (Fig. 1*D*) confirms structurally the successful alignment and contact of the two layers.

An optical micrograph of a region of a typical 3D NW CMOS chip (Fig. 2*A*) shows both isolated n- and p-FETs (Fig. 2*A*, left

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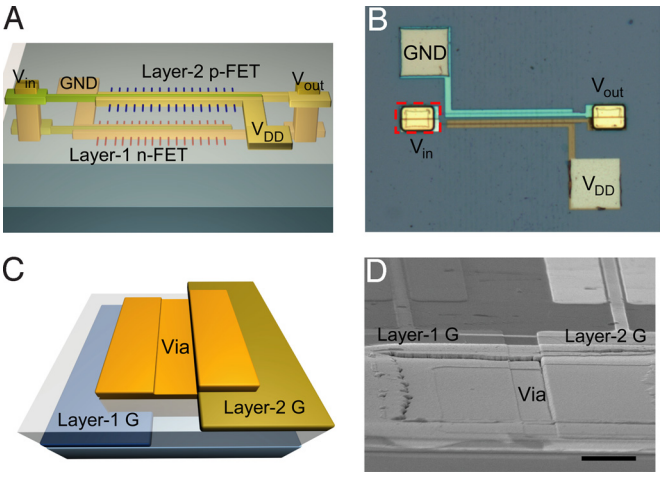


**Fig. 1.** The 3D CMOS circuit and vertical interconnection. (*A*) Schematic of a two-layer CMOS inverter circuit. Layer-1 and layer-2 are constructed with complementary n-type InAs NWs and p-type Ge/Si core/shell NWs, and vertical interconnections are achieved at the two gate electrodes (input) and the two drain electrodes (output). GND denotes electrical ground. (*B*) Optical microscope image of vertically interconnected CMOS inverter. Red dashed box indicates via interconnection at the input of CMOS inverter. (*C*) Side tilted-view schematic drawing (rotated 90° counterclockwise of red dashed box in *B*) of via interconnection at the input of CMOS inverter. (*D*) Tilted-view SEM image (rotated 90° counterclockwise of red dashed box in *B*) of via interconnection at the input of CMOS inverter. (Scale bar: 5 $\mu$m.)

column) and inverter logic gates (Fig. 2*A*, right column). The isolated NW FETs were used to characterize sequentially during fabrication the properties of InAs NW n-FETs and then Ge/Si NW p-FETs. Representative transfer characteristics of layer-1 InAs NW n-FETs and layer-2 Ge/Si NW p-FETs (Fig. 2*B*) show that the n- and p-FETs have similar current levels, with values of 23 and 15 $\mu$A, respectively, where $|V_{gs}| = 1$ V and $|V_{ds}| = 1$ V (see Figs. S1 and S2 full device characterization data). We note that the current levels can be readily adjusted by varying the average number of NWs/FET deposited during the printing/deposition step. Furthermore, the intersection point of the two $I$–$V_g$ transfer curves, ≈0.5 V, corresponds to the ideal value of $V_{DD}/2$, where $V_{DD} = 1$ V is the supply voltage for both FETs (22). DC characterization of the $V_{out}$ versus $V_{in}$ response for a corresponding vertically interconnected CMOS inverter for $V_{DD} = 4$ V (Fig. 2*C*) shows a sharp switching at ≈2.2 V, near the ideal value of $V_{DD}/2$. The derivative of the data shows a substantial DC gain of ≈45. This gain and the rail-to-rail output switching are consistent with the large noise margin and minimal static power consumption, key characteristics of CMOS (22).

This representative result from the 3D CMOS inverters is a significant improvement over the corresponding 3D but pMOS-only inverter, consisting of a p-Ge/Si NW switching FET (layer-1) and a p-Ge/Si NW load FET (layer-2) (Fig. S3), which was constructed for comparison. The pMOS-only inverter has a DC gain of only ≈8 and a nonideal switching threshold of ≈3 V at supply voltage of 4 V. Notably, the nearly ideal behavior, achieved for the 3D CMOS NW inverter, suggests that our bottom-up vertical interconnection approach of high-performance III-V InAs NW n-FET and IV Ge/Si NW p-FETs can be used to realize more complex CMOS integrated circuits.

To demonstrate the potential to extend our approach to more complex vertically interconnected, 3D CMOS circuits, we have also fabricated two-layer, three-stage CMOS ring oscillators. An optical micrograph and circuit schematic (Fig. 3*A*) highlight the three CMOS inverters serially connected in a closed, positive feedback loop, with each inverter consisting of a layer-1 InAs NW n-FET and a layer-2 Ge/Si NW p-FET, which are vertically

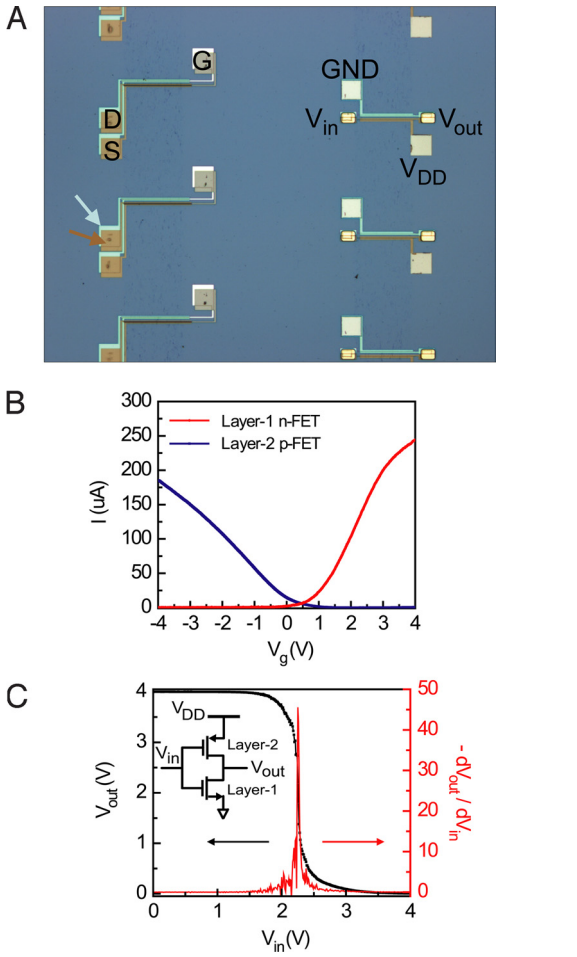


**Fig. 2.** Vertically interconnected CMOS inverter. (*A*) Optical microscope image of isolated n-InAs and p-Ge/Si NW FETs (left column), and two-layer interconnected CMOS inverters (right column). The n-InAs NW FETs were fabricated in layer-1 (light-blue contrast and arrow), and the p-Ge/Si NW FETs were fabricated in layer-2 (light-brown contrast and arrow). (*B*) $I$ vs. $V_g$ characteristics data recorded from representative InAs layer-1 and Ge/Si layer-2 NW devices with $|V_{ds}| = 1$ V. The data from the InAs NW FET were recorded before fabrication of the layer-2. (*C*) $V_{out}$ vs. $V_{in}$ (black curve) and gain = $dV_{out}/dV_{in}$ vs. $V_{in}$ (red curve) for a CMOS inverter at supply voltage, $V_{DD}$, of 4 V. (*Inset*) Circuit diagram for the vertically interconnected two-layer CMOS inverter.

interconnected. Significantly, measurement of the output signal with a high impedance probe (see *Materials and Methods*) demonstrates stable, self-sustained oscillations with a maximum frequency of 108 MHz for $V_{DD} = 8$ V, as shown in Fig. 3*B*. This oscillation frequency corresponds to a propagation delay of 1.54 ns per stage and is nearly an order of magnitude improvement from the pMOS-only ring oscillator (≈12 MHz; Fig. S4), which we fabricated for comparison. The substantially higher oscillation frequency or decreased inverter delay is due to the larger current-driving capability of the CMOS inverter, in comparison to the pMOS-only inverter. In addition, a higher range of oscillation frequencies, 330–490 MHz, was estimated for our 3D CMOS ring oscillator based on an inverter propagation delay calculation (see *SI Text*). This analysis suggests that parasitic components of the circuit may be major sources of delay in our experimental results, although future studies focused on detailed circuit simulations may provide further insights on how to improve the performance of our 3D NW-based circuits. Last, our measurements demonstrate that the oscillation frequency and output voltage swing increase with supply voltage (Fig. 3*C*),

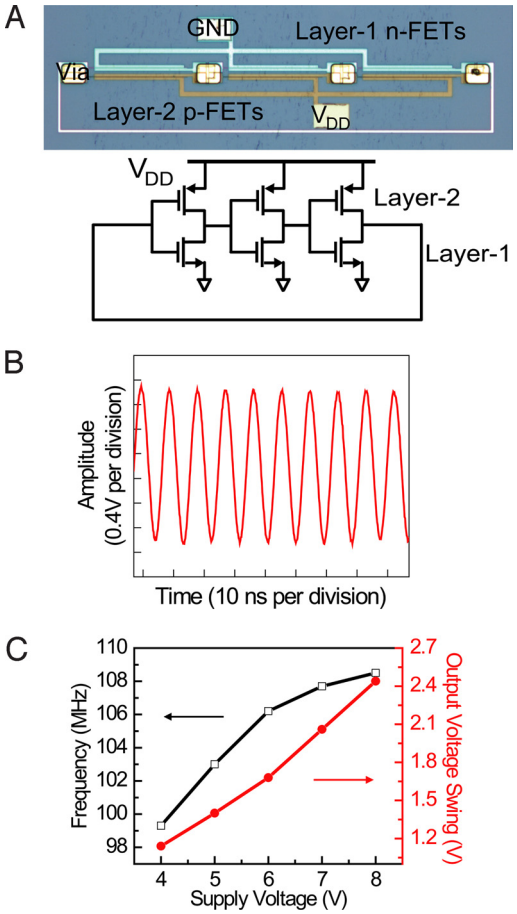


**Fig. 3.** Vertically integrated CMOS ring oscillator. (*A*) Optical micrograph and circuit diagram of two-layer, vertically interconnected three-stage CMOS ring oscillator. The layer-1 n-InAs and layer-2 p-Ge/Si NW FETs exhibit light-blue and brown contrast in the image. (*B*) Amplitude vs. time response recorded at via position by using a high-impedance probe (see *Materials and Methods*). The supply voltage, $V_{DD}$, is 8 V, and the self-sustained oscillation frequency is 108 MHz. (*C*) Oscillation frequency (black curve) and output voltage swing (red curve) vs. supply voltage ($V_{DD}$) characteristics of the vertically interconnected three-stage CMOS ring oscillator.

showing that these vertically interconnected NW circuits behave as expected for conventional oscillator circuit (22). It is also important to note that the yield of vertically interconnected NW ring oscillators was 80%; of 28 circuits fabricated and tested, 23 were functional. We believe that this represents an important achievement in comparison to previous studies of electronic devices and circuits based on synthesized nanostructures.

These results can be compared to the two previous studies (9, 10) of 3D integrated circuits using nanomaterials. The work in ref. 10 demonstrated layer-by-layer assembly of NW p-FETs, but neither vertical interconnection nor CMOS configuration was achieved. In an important advance, Rogers and coworkers (9) first demonstrated a 3D CMOS inverter based on vertically interconnected n-type Si micrometer-scale ribbon and p-type network single-walled nanotube FET device layers (9). However, these initial studies also had limitations, including nonideal switching, which precludes achieving full advantage of CMOS operation, and substantially lower gain (≈8) than we achieved by using matched high-performance p-Ge/Si and n-InAs NW FETs. In addition, circuits more complex than inverters were not constructed, and AC operation capability, which is essential in almost all practical applications and represents a key advance of the present ring oscillators, was not demonstrated.

In addition, we can compare the high-frequency ring-oscillator performance to previous, less-demanding 2D structures. In particular, work on single CNT-based CMOS ring oscillators (23, 24) achieved, before our work, the highest oscillation frequency, ≈72 MHz, for nanomaterial-based integrated circuits. However, the ambipolar nature of the CNT FETs used to configure inverter elements could cause relatively large leakage currents and nonideal noise margins compared to our NW CMOS inverter units, making fabrication of more complex high-performance circuits increasingly difficult. More importantly, we believe that 3D integration demonstrated in present work represents a key advance for exploring interesting and unique high-performance nanomaterial-based CMOS circuits for the future.

## Conclusions

We have demonstrated fully functional 3D CMOS NW integrated circuits based on sequential layer-by-layer assembly of chemically synthesized high-performance NW building blocks followed by interconnection of layers to define final circuits. More specifically, we have used interconnected layer-1 InAs NW n-FETs and layer-2 Ge/Si NW p-FETs to demonstrate 3D CMOS inverters with well-controlled switching thresholds and DC gains up to 45, as well as 3D CMOS ring oscillators with oscillation frequencies up to ≈110 MHz. Our 3D ring oscillator represents the highest-frequency integrated circuit reported for nanoscale materials, and we believe this frequency could be further increased by reducing channel length and parasitic resistance and capacitance of the circuit. More generally, we believe that our bottom-up approach using optimized n- and p-type NW materials suggests substantial promise for several directions, including (*i*) extension to multiple interconnected layers both for increasing device packing density (1, 2) and to open up design and testing of novel circuit architectures (1, 2), (*ii*) implementation of 3D interconnected NW circuits on flexible (25–28) and highly curved substrates (29) for high-performance electronics on unconventional substrates, and (*iii*) exploring general concept of heterogeneous 3D integration of two or more NW and carbon nanotube building blocks for 3D multi-functional nanosystems (11).

## Materials and Methods

**Synthesis of Ge/Si and InAs NWs.** Epitaxial core/shell Ge/Si NW heterostructures were prepared by the nanocluster catalyzed vapor–liquid–solid (VLS) growth process by using germane and silane reactants as described previously (19). A core diameter of ≈10 nm and a uniform shell thickness of ≈2 nm were used. InAs NWs were grown by the nanocluster catalyzed VLS method using thermal evaporation and transport in a two-zone tube furnace to deliver precursors. Briefly, several grams of InAs powder (99.9999%; Alfa Aesar) was placed in zone I (upstream), and a $Si/SiO_2$ substrate with dispersed 10 nm gold nanoparticles (Ted Pella) was placed 20 cm downstream in zone II of the tube furnace. Temperatures were set to 690 °C (zone I) and 530 °C (zone II), with a total pressure maintained at 2 torr in a 20 standard cubic cm per min flow of $H_2$ gas. Single-crystalline InAs NWs with diameters of ≈20 nm were obtained after 40 min of growth. Independent tuning of source and substrate temperature together with pressure and gas flow were found to be important for realizing controlled synthesis of uniform InAs NWs with improved off-current levels and subthreshold slopes (18).

**Contact Printing of NWs.** NWs were transferred from growth substrates to patterned device substrates by a shear printing process, which enables control of the density and alignment of the NWs. First, device substrates (600 nm $SiO_2$ on intrinsic Si) were patterned by photolithography (Shipley S1805) to define the regions where NWs will be deposited (Fig. S5*A*). The average number of NWs, or NW density, was controlled by adjusting the photoresist trench width and spacing. The trench width and spacing was 4 $\mu$m for InAs NWs and 2 $\mu$m for Ge/Si NWs; the values were chosen to match the on-current levels of n- and p-type NW FETs. Second, an NW growth substrate was brought into contact with the patterned device substrate (NWs facing the device substrate). A pressure of 0.5–1 kg/cm$^2$ was applied while the NW substrate was slid by 1–3 mm (Fig. S5*B*). Last, the photoresist layer on device substrate was lifted off in acetone (Fig. S5*C*). These procedures produced relatively low-density NW arrays: InAs ≈0.1 NW per micrometer and Ge/Si ≈0.2 NW per micrometer.

**Multilayer NW Circuit Fabrication.** InAs and Ge/Si NWs were contact-printed onto $Si/SiO_2$ (60,000–160,000 Ω·cm intrinsic Si substrate/600 nm thermal oxide; Nova Electronic Materials) substrate with patterned photoresist spacer layers (10). Ge/Si NWs were printed on the first layer of the interconnected two-layer pMOS circuit, and InAs NWs were printed on the first layer of the interconnected two-layer CMOS circuit. S/D electrodes were patterned by photolithography followed by metallization with Ni (60 nm thickness). A channel length of 1.5 $\mu$m and channel width of 200 $\mu$m were used as standard FET dimensions, with the NW density adjusted by contact printing. Buffered HF (Transene) and diluted HF (48% HF:deionized water = 1:1,000) solutions were used in ≈3 s etch of the contacts for the Ge/Si and InAs NWs, respectively, immediately before contact metal deposition. Subsequently, the top-gate high-$\kappa$ dielectric $HfO_2$ film (≈20 nm) was deposited by 150 cycles of ALD at 115 °C, with each cycle consisting of 1 s water-vapor pulse, 5 s $N_2$ purge, 3 s tetrakis(dimethylamino)hafnium [$Hf(N(CH_3)_2)_4$] pulse, and 5 s $N_2$ purge steps. Cr/Au (5 nm/55 nm) and Ti (100 nm) top-gate metals were evaporated for InAs n-FETs and Ge/Si p-FETs, respectively.

After fabrication of first-layer devices, a $SiO_2/HfO_2$ (300/20 nm) bilayer was deposited to electrically isolate the second device layers, where the $HfO_2$ layer served as a convenient barrier for the contact etching step. The second-layer FET fabrication followed steps similar to the first layer: contact-printing Ge/Si NWs, S/D and top-gate fabrication steps. Practically, the second layer devices were offset by 20 $\mu$m to avoid any roughness from first-layer fabrication, although we note that standard surface planarization techniques (30) could eliminate this roughness and eliminate the need for the small offset. Last, the upper and lower layers were interconnected. Via holes were formed by removing oxide layers by $CF_4$ reactive ion etching dry-etching process with a double-layer LOR3A/S1813 photoresist as an etch mask, and Cr/Au was then deposited by sputtering to achieve electrical interconnection. We used a surface-contact strategy by designing non-overlapping metal electrodes at via interconnection points (Fig. S6).

**Device Measurements.** Measurements were conducted with a probe station (model 12561B; Cascade Microtech) and a semiconductor parameter analyzer (model 4156C; Agilent). Inverter DC measurements were carried out by using a computer-controlled analogue-to-digital converter (model 6030E; National Instruments). Ring-oscillator output voltage was monitored by an oscilloscope (model TDS3012; Tektronix) using a 10 MΩ impedance FET probe (model 34A; Picoprobe), with DC bias voltage applied to the circuit. A bias tee (MiniCircuits) was used between the oscilloscope and high-impedance probe to monitor only high-frequency signals from the ring-oscillator circuit. The 20:1 signal reduction intrinsic to the probe was compensated for in the data presented in Fig. 3 and Fig. S4.

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