Supporting Information

Nam et al. 10.1073/pnas.0911713106

SI Text

Estimation of Oscillation Frequency. The inverter propagation delay can be estimated based on

$$t = \frac{C_L V_{DD}}{2 I_d}, \quad [1]$$

(ref. 1), where C_L is load capacitance, V_{DD} is supply voltage, and I_d is drain current.

$$\frac{V_{DD}}{I_d} \approx \frac{8V}{800\ \mu A} = 10k\Omega, \quad [2]$$

where the value of I_d corresponds to either n- or p-type NW FET in the CMOS inverter when V_{DD} is 8 V. We assume that the top-gate capacitance (C_G) and parasitic capacitance of the measurement probe (C_{probe}) are the two major sources of load capacitance (C_L). A range of C_G values was estimated based on the cylindrical capacitor model (2).

$$\frac{C_G}{L} = \frac{2\pi\epsilon\epsilon_0}{\ln\left[\frac{b}{a}\right]}, \quad [3]$$

where a is the radius of NW, b is the radius of NW plus high-κ dielectric, ε is the dielectric constant ($\varepsilon = 20$ for HfO_2), and L is the gate channel length ($L = 1.5\ \mu$m). The upper limits of the capacitance values for the Ge/Si and InAs NWs, 0.87 and 1.52 fF, correspond to a full cylindrical gate, and the lower bounds would be the capacitance of the half-cylinders, 0.44 and 0.76 fF, respectively. Assuming 40 Ge/Si NWs and 20 InAs NWs are in each channel, estimated top-gate capacitance range is between ≈33 fF and ≈66 fF. The value of C_{probe} was 100 fF (model 34A; Picoprobe).

Substituting the values from Eq. **3** into Eq. **1** with $C_G = C_L$ yields inverter propagation delays, t_d, between 0.17 and 0.33 ns, which correspond to delays in two inverter stages (t_1 and t_2)

$$t_1 = t_2 = t_d = \frac{C_G V_{DD}}{2 I_d}. \quad [4]$$

The delay in the remaining inverter stage (t_3), whose output is connected to the measurement probe is

$$t_3 = t_d + t_{probe} = \frac{V_{DD}}{2 I_d}(C_G + C_{probe}), \quad [5]$$

where C_G is in parallel connection with the probe capacitance (C_{probe}). The t_3 ranges between 0.67 and 0.83 ns.

Finally, these delay times can be used to estimate the oscillation frequency (f) of our three-stage ring oscillator by using (1)

$$f = \frac{1}{2\cdot(2t_1 + t_3)}, \quad [6]$$

which gives oscillation frequency values from 336 to 495 MHz.

1. Taur Y, Ning TH (2005) *Fundamentals of Modern VLSI Devices* (Cambridge Univ Press, New York).

2. Wolfson R, Pasachoff JM (1994) *Physics for Scientists and Engineers* (HarperCollins College, New York).

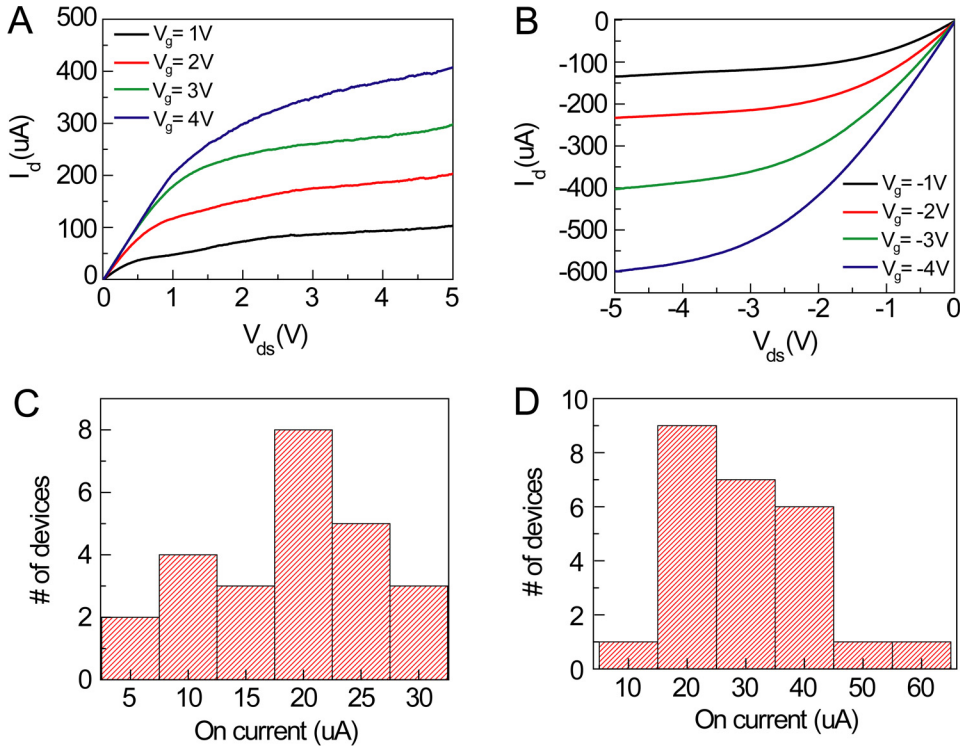

Fig. S1. n-InAs and p-Ge/Si NW FETs IV characteristics and statistical variations of on current levels. (*A* and *B*) Drain current (I_d) vs. drain-source voltage (V_{ds}) characteristics of an n-type InAs and a p-type Ge/Si NW FET, respectively. The data presented here are from similar but not identical devices, as shown in Fig. 2*B*. (*C* and *D*) Statistical variations of the on current levels of n-InAs (*C*) and p-Ge/Si NW FETs (*D*), when $|V_{gs}| = 1$ V and $|V_{ds}| = 1$ V. Average on current ± 1 SD of n-InAs and p-Ge/Si NW FETs are 18.8 $\pm$ 7.2 μA and 30 $\pm$ 11.3 μA, respectively.

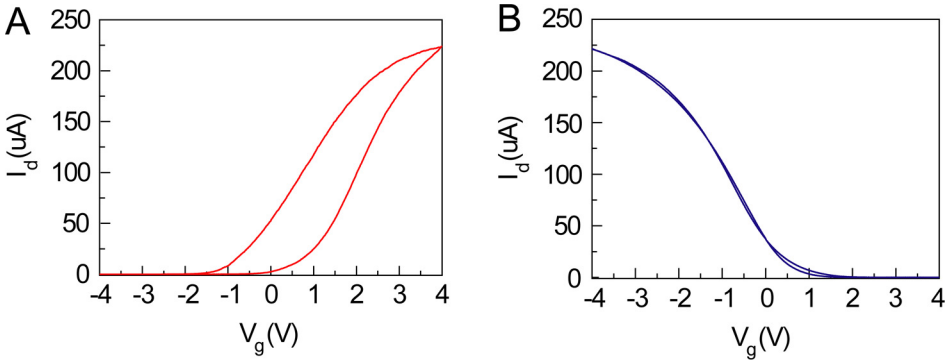

Fig. S2. DC transfer characteristics of n-InAs and p-Ge/Si NW FETs with bidirectional gate sweeps. (*A*) Drain current vs. gate voltage characteristics of n-InAs NW FET with forward and backward gate sweeps, when $V_{ds} = 1$ V. (*B*) Transfer characteristics of p-Ge/Si NW FET with bidirectional gate sweeps, when $V_{sd} = 1$ V. The data presented here are from similar but not identical devices, as shown in Fig. 2*B* and Fig. S1. The Ge/Si NW FET exhibits very little hysteresis and is typical of all of these NW FETs. In contrast, the InAs NW FETs typically exhibit hysteresis, as in *A*. The hysteresis, which is believed to arise from surface charge traps, will tend towards zero as operation frequency exceeds the charge-hopping frequency.

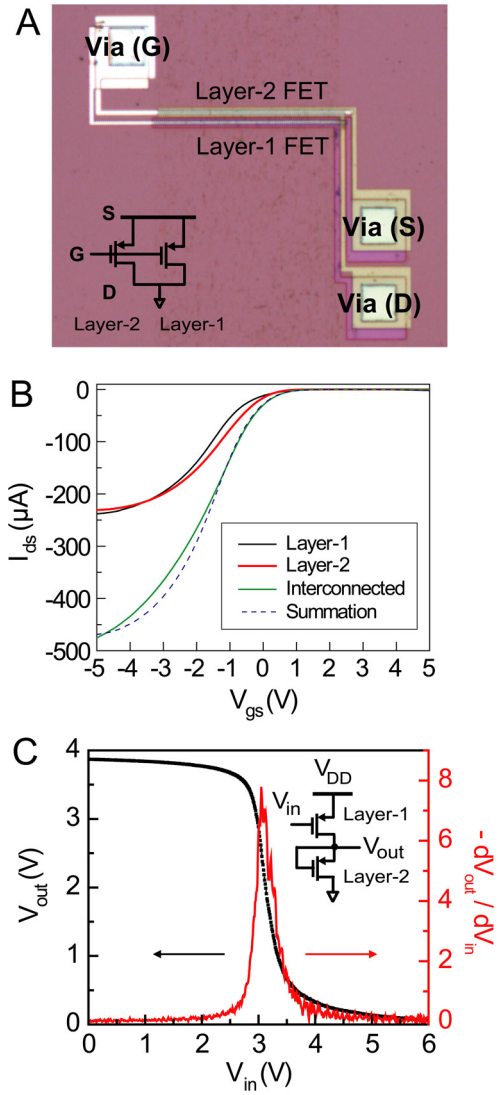

Fig. S3. Vertically interconnected pMOS FETs and inverter. (*A*) Optical microscope image of two-layer interconnected pMOS NW FET. Both layer-1 and layer-2 devices are fabricated by using Ge/Si p-type NWs. (*Inset*) Circuit schematic for the parallel connection of the p-FETs in the two layers. (*B*) I–V_{gs} characteristics of the two-layer Ge/Si p-FETs before (black and red curves) and after interconnection (green curve) at $V_{ds} = -1$ V. The dashed line corresponds to a summation of the black and red curves recorded from layer-1 and layer-2 NW FETs before interconnection. (*C*) V_{out} vs. V_{in} characteristics (black curve) and gain = dV_{out}/dV_{in} vs. V_{in} (red curve) characteristics of a pMOS inverter at supply voltage of 4 V. (*Inset*) Circuit diagram of two-layer pMOS inverter.

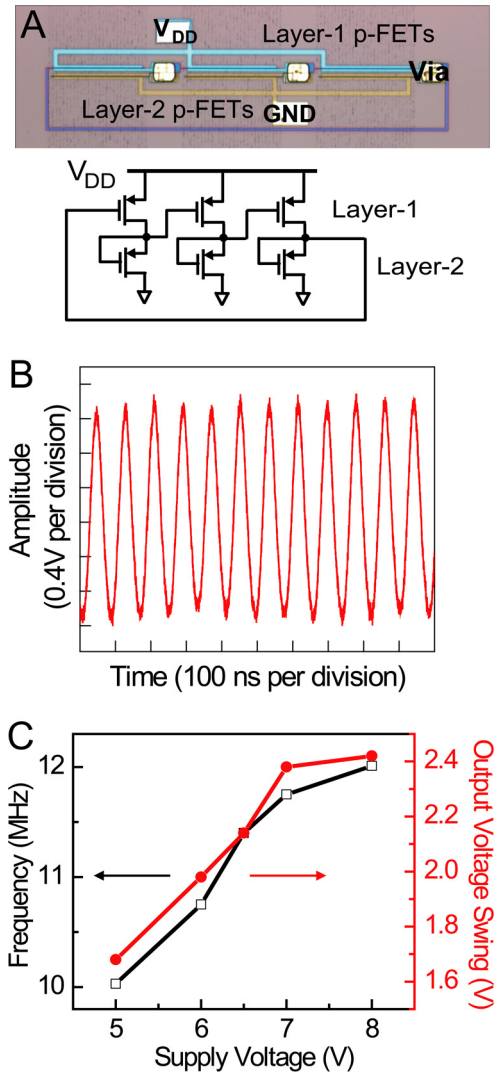

Fig. S4. Vertically integrated pMOS ring oscillator. (*A*) Optical microscope image of a two-layer, interconnected three-stage pMOS ring oscillator, where the layer-1 and layer-2 structures exhibit light-blue and brown contrast, respectively. The corresponding circuit schematic for the two-layer interconnected pMOS ring oscillator is shown. (*B*) Amplitude vs. time response recorded at via position by using a high-impedance probe. The supply voltage, V_{DD}, is 8 V, and the self-sustained oscillation frequency is 12 MHz. (*C*) Oscillation frequency (black curve) and output voltage swing (red curve) vs. supply voltage (V_{DD}) for the two-layer, three-stage pMOS ring oscillator.

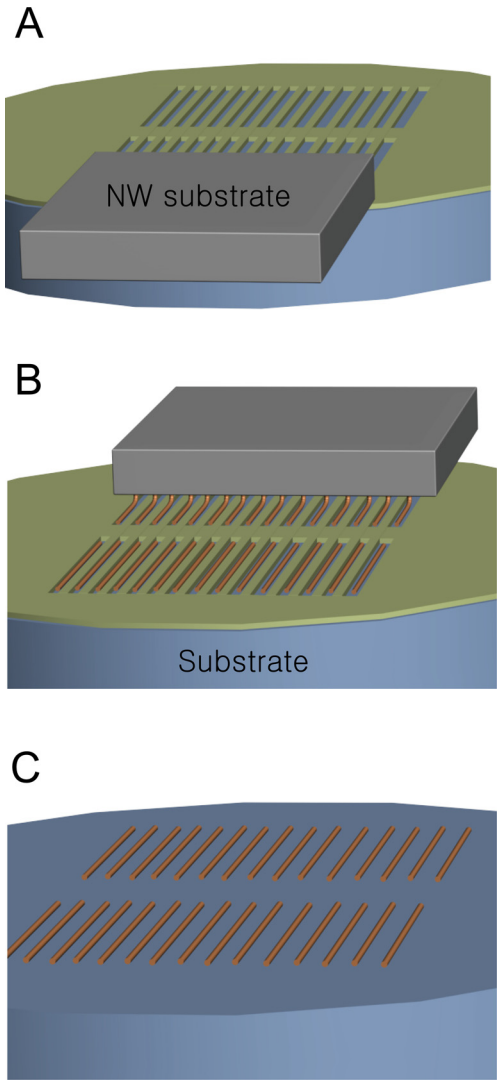

Fig. S5. Contact printing of NWs from growth substrate to patterned device substrate. (*A*) Schematic drawing showing NW growth substrate placed upside down on top of photoresist patterned device substrate. The NW density can be controlled by adjusting the photoresist trench width and spacing. (*B*) NWs are transferred from growth substrates to patterned device substrates by a shear printing process. Topside pressure of 0.5–1 kg/cm^2 and a travel distance of 1–3 mm are typical process parameters. (*C*) Aligned arrays of NWs with controlled density are realized after photoresist liftoff.

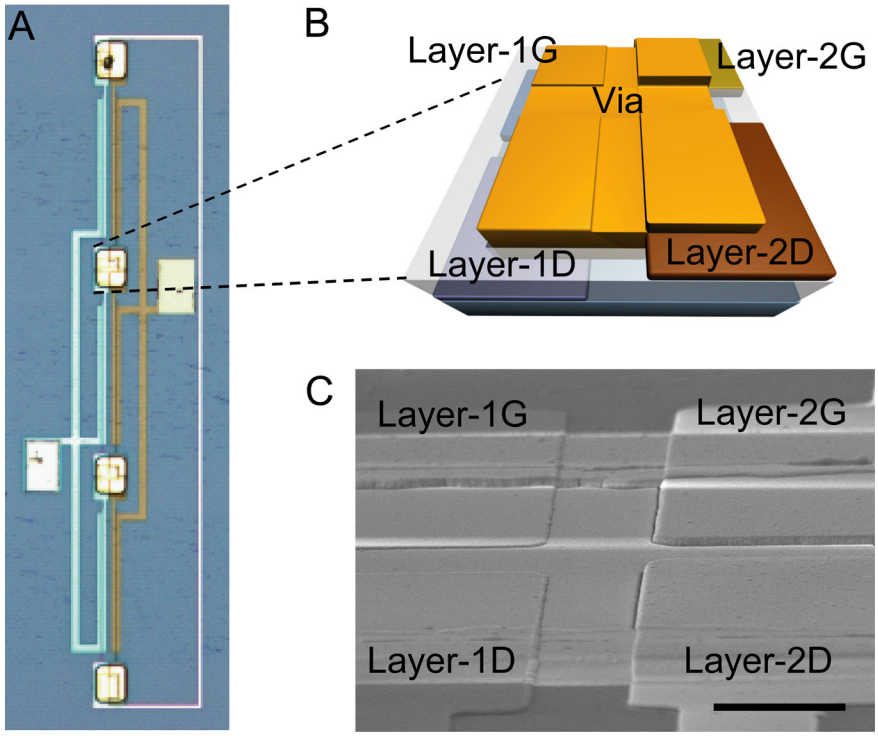

Fig. S6. Via interconnection strategy in CMOS ring-oscillator circuits. (*A*) Optical microscope image of CMOS ring-oscillator circuit. (*B*) Side tilted-view schematic drawing of via interconnection showing non-overlapping of metal electrodes at different layers. (*C*) Tilted-view SEM image of via interconnection. (Scale bar: 5 μm.)