Supporting Information

Electrochemical Deposition of Conformal and Functional Layers on High Aspect Ratio Silicon Micro/Nanowires

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Materials and chemicals

All chemicals and solutions were used without further processing. Silicon wafers (4′′ <100> 1-10 ohm/cm p-type, 4′′ <100> 0.001–0.005 ohm/cm p-type, 4′′ <100> 0.001-0.005 ohm/cm n-type) were purchased from Nova Electronic Materials. Commercially available plating solutions (Cyless for Ag, Orotemp 24 Rack for Au, Copper C for Cu, nickel sulfamate for Ni, Techni Rhodium for Rh, Ruthenium U for Ru, and Pallaspeed VHS for Pd) were purchased from Technic Inc. Ammonium hexachloroplatinate (99.999%), sodium phosphate dibasic (99%), manganese(II) acetate (≥99), iron(II) sulfate heptahydrate (≥99%), cobalt(II) nitrate hexahydrate (≥98%), boric acid (≥99.5%), ascorbic acid (USP Standard), sodium acetate (≥99%), cadmium sulfate (99%), selenium dioxide (99.9%), cadmium chloride (99.99%), sulfur (≥99.5%), dimethyl sulfoxide (≥99%), lithium perchlorate (99.99%), pyrrole (98%), aniline (99%), 3,4-ethylenedioxythiophene (97%), concentrated perchloric acid (≥99.999%), potassium hydroxide (≥99%), nitric acid (ACS grade), sulfuric acid (ACS grade), and iron(III) chloride (97%), were purchased from Sigma Aldrich. SU-8 2005 photoresist, S1800 series photoresists and their developers were purchased from MicroChem. Buffered Oxide Etch 7:1 (BOE) was purchased from J. T. Baker. Au nanoparticle solutions were purchased from Ted Pella.

Instrumentation

Wet oxidation was completed with a Tystar Tytan 4600 wet/dry oxide furnace. Scanning transmission electron microscope (STEM) and transmission electron microscope (TEM) images were acquired using a JEOL ARM-200 STEM. STEM elemental mapping was conducted with an EDAX detector. Scanning Electron Microscope (SEM) images were acquired using Zeiss Supra55, Ultra55, and Ultra Plus SEMs. STEM and SEM elemental mapping were conducted with EDAX detectors. Electrochemical deposition of metals and inorganic semiconductors were done using a Gamry Instruments Interface 1000 potentiostat. Argon reactive ion etching (RIE) was completed with a Nexx RIE system. Deep reactive ion etching (DRIE) for the fabrication of high aspect ratio structures was completed with a SPTS Rapier DRIE system. Photolithography was performed using a Karl Süss MJB4 mask aligner.

Top-down nanowire fabrication

Nanowires were fabricated in a conventional top-down method. Briefly, a layer of SU-8 2005 (SU-8 2002 in some samples) was spin-coated on a silicon wafer at 500 rpm for 10 s and 3000 rpm for 60 s. The resist was pre-baked at 65 °C and 95 °C for 2.5 and 5 min, respectively. The resist was patterned by exposing the resist through a mask with 1.5–2 μm diameter holes using a mask aligner. The resist was post-baked at 65 °C and 95 °C for 2.5 and 5 min, respectively. The patterns on SU-8 were then processed in SU-8 developer solution for 1 min leaving an array of circular SU-8 spots. The resist was then baked a final time at 180 °C for 20 min. The wafer was then etched in a DRIE (SPTS Rapier) to yield an array of microwires. Wire thinning was completed by growing a wet oxide layer around the microwires at 1000 ºC and subsequent etching of the oxide in BOE

at room temperature. The desired wire aspect ratio was achieved by controlling the DRIE etching (height) and wet oxide formation (diameter).

Bottom-up nanowire growth

A 5 mL solution of Au nanoparticle catalysts (100 nm diameter) was mixed with 0.5 mL of 49% HF solution and the particles were subsequently dispersed onto a Si growth chip. After rinsing in deionized water and drying with nitrogen, the substrates were placed into a home-built chemical vapor deposition reactor and the system was evacuated to a base pressure of ~5 mTorr. Si nanowires were grown via the Au nanoparticle catalyzed growth mechanism (Reference 22 of main text) for ~30 min at 475 °C and a total pressure of 10 Torr with 1 standard cubic centimeter per second (sccm) silane (SiH_4, 100%, Voltaix), 60 sccm hydrogen (H_2, 99.999%, Matheson), and 3 sccm of diborane (B_2H_6, 100 ppm in H_2, Voltaix) flow rates.

Electrodeposition procedures

Unless mentioned otherwise, a conventional three-electrode electrochemical cell positioned in a Teflon cell was used for the electrodeposition of materials with a Pt counter electrode, an Ag/AgCl reference electrode, and the Si wire array as the working electrode. A diamond tip pen was used to scratch the surface of the silicon to facilitate better electrical contact. Prior to electrodeposition, Si wire arrays were submerged in BOE in order to etch any native oxide that forms on the surface of silicon. The electrochemical cell and electrodes were thoroughly washed in nanopure water after each deposition step(s).

Metals were deposited at constant potential from the following aqueous solutions:

Table S1. Applied potentials and electrolyte solutions used in metal depositions.

Metal	E_{appl}/mV	Solution
Au	–930	Orotemp® 24 RTU Rack (Potassium aurocyanide 1.0%)[a]
Ag	–800	Techni Silver® Cyless® II RTU (Potassium hydroxide 7%, Silver oxide 2.4%)
Cu	–1400	Copper C RTU (Potassium copper cyanide 16%, Potassium hydroxide 2%)[a]
Fe	–1050	54 mM $FeSO_4$, 0.5 M H_3BO_3, 3 mM ascorbic acid
Ni	–900	High Speed Nickel Sulfamate FFP RTU (Nickel sulfamate 30%, Nickel bromide 0.7%, Boric acid 3%)
Rh	–500	Techni Rhodium (2.1 g/l Rh)
Ru	–1000	Ruthenium U (Sulfamic acid 6%, Ruthenium chloride 1.4%)
Pd	–900	Pallaspeed VHS (Palladium ethylenediamine sulfate 3.97%)
Pt	–650	15 mM $(NH_4)_2PtCl_6$ and 200 mM Na_2HPO_4

[a] *Caution*: solution contains cyanide

Metal oxides were deposited at constant potential from the following aqueous solutions:

Table S2. Applied potentials and electrolyte solutions used in metal oxide depositions.

Oxide	E_{appl}/mV	Solution
MnO_x	+1000	14 mM manganese acetate
CoO_x	+1050	0.5 mM cobalt(II) nitrate, 50 mM sodium acetate

Polymerizations were performed at constant potential from the following solutions:

Table S3. Applied potentials and electrolyte solutions used in polymer depositions.

Polymer	E_{appl}/mV	Solution
Polypyrrole (PPy)	+900	510 µL pyrrole in 30 mL of 0.1 M $LiClO_4$
Polyaniline (PANI)	+1000	680 µL aniline in 15 mL of 0.1 M $HClO_4$
Poly-3,4-ethylene-dioxythiophene (PEDOT)	+900	15 µL 3,4-ethylenedioxythiophene in 10 mL of 0.1 M $LiClO_4$

Chalcogenides were deposited electrochemically as previously reported using the following solutions:

Table S4. Applied potentials and electrolyte solutions used in chalcogenide depositions.

Chalcogenide	Method	Conditions	Solution
CdSe	cyclic voltammetry	–400 to –800 mV vs SCE at 100 mV/s	0.7 mM SeO_2, 0.3 M $CdSO_4$, 0.25 M H_2SO_4, Triton X (0.25% v/v)
CdS	constant current	–1.5 mA cm^{-2} at 130 °C, 2-electrode configuration	1.52 g of $CdCl_2$, 914 mg of S in 150 mL of 130 °C DMSO

Deposition of core-shell structures

Core-shell structures were deposited by sequential electrodeposition. Alternating layers of Ni and Au were deposited sequentially on the Si wire array. The tips of the wires were cleaned by physical etching using Ar RIE etching. Finally, selective etching of Ni with a 3% w/w aqueous solution of $FeCl_3$ affords Au-Si core-gap-shell structures.

Selective removal of wire tips

Si wire tips were cleaned after electrodeposition with isotropic Ar RIE. A typical RIE process involves 5 min of etching with 20 sccm of Ar flow and 400 W of applied DC power and 200 W of applied RF power at 5 mT pressure. The amount of wire tip etched is controlled by the etch time.

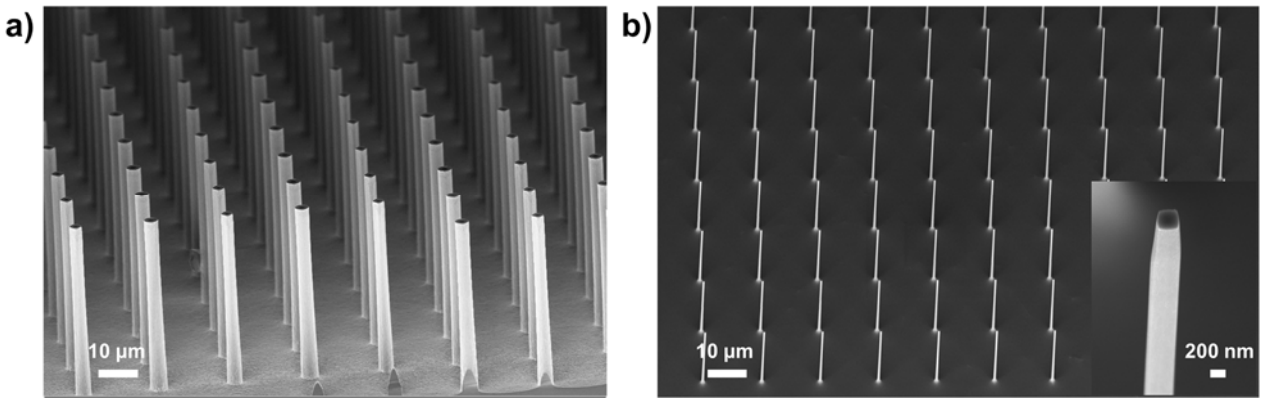

Figure S1. Scanning electron microscope images of top-down fabricated, bare Si a) microwire and b) nanowire wire arrays.

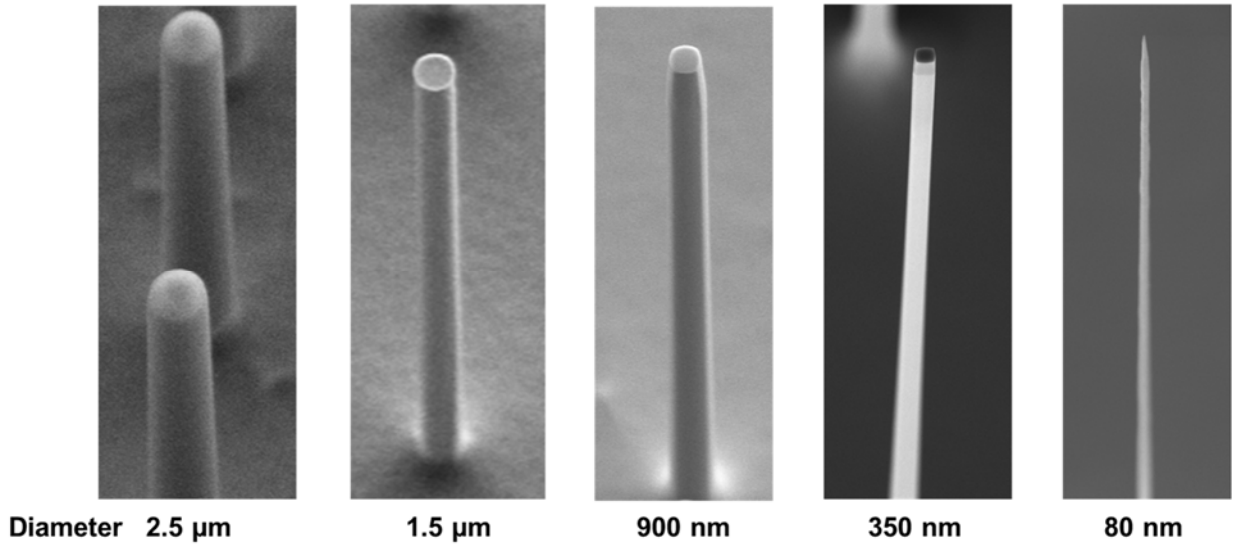

Figure S2. Scanning electron microscope images of wires showing progressive reduction in wire diameter. Extended high temperature exposure in a wet oxide furnace from 1 h to 10 h and consequent oxide etch results in thinned wire arrays.

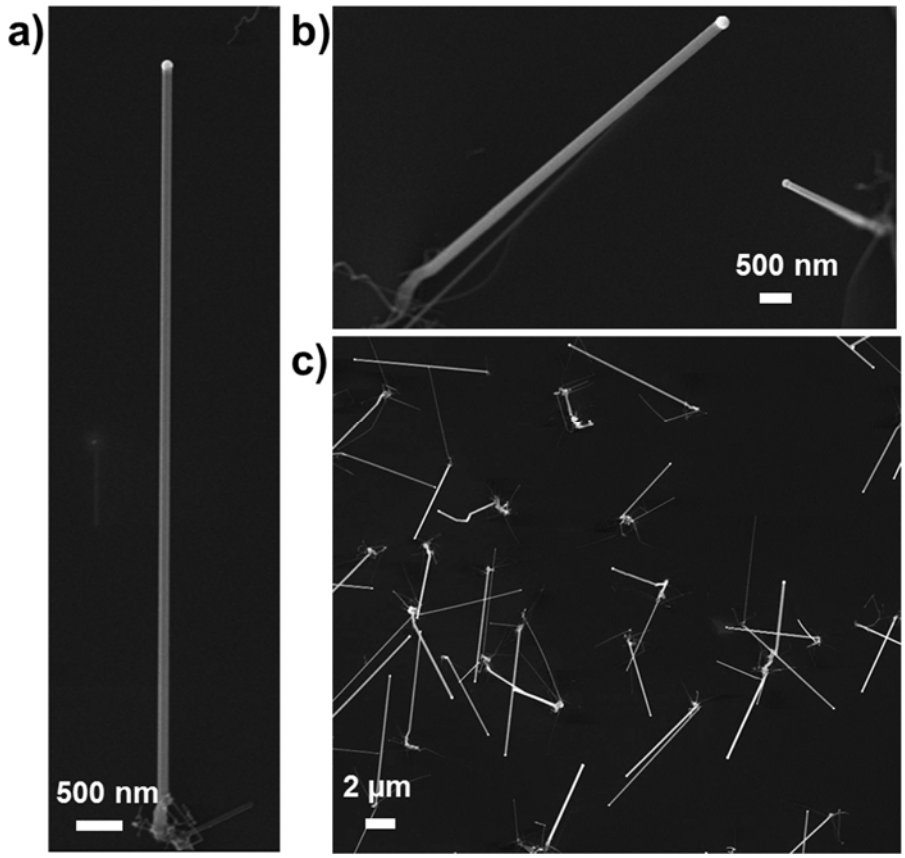

Figure S3. Scanning electron microscope images of bottom-up grown wires showing growth of high aspect ratio wires (a and b) in random orientations (c).

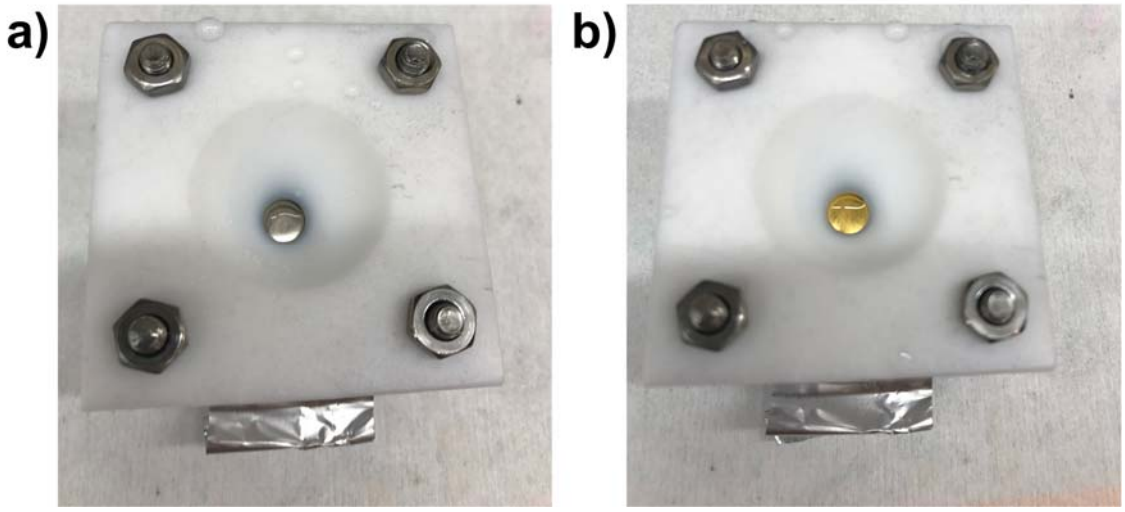

Figure S4. Photographs of nanowire arrays (positioned in the middle of the Teflon cell) after deposition of a) Ni and b) Au layer. For small silicon chips, electrical contact can be made with carbon tape bridging the scratched silicon surface and aluminum foil.

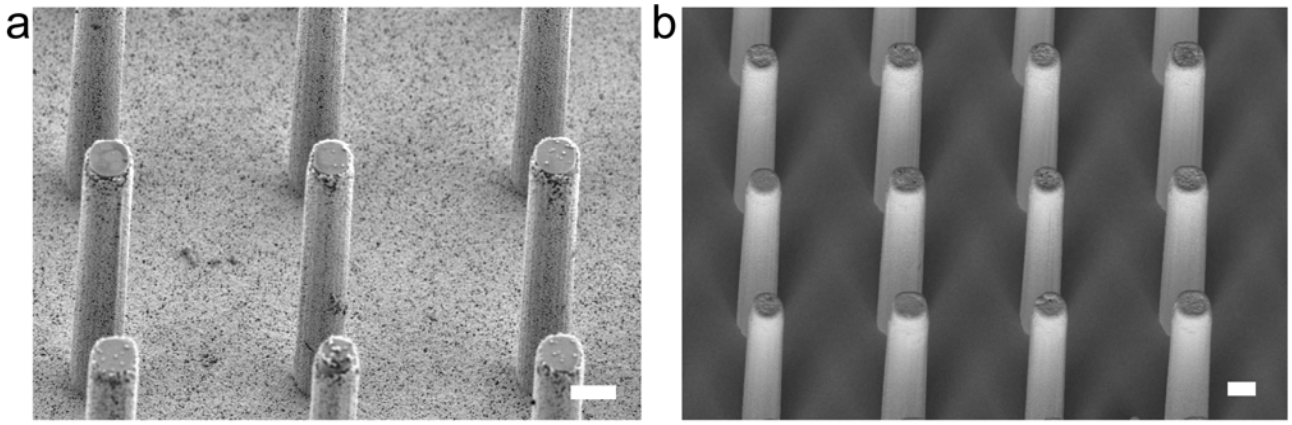

Figure S5. Scanning electron microscope images of (a) Au nanoparticles and (b) continuous Au film around low conductivity Si wires. Scale bars equal 2 μm.

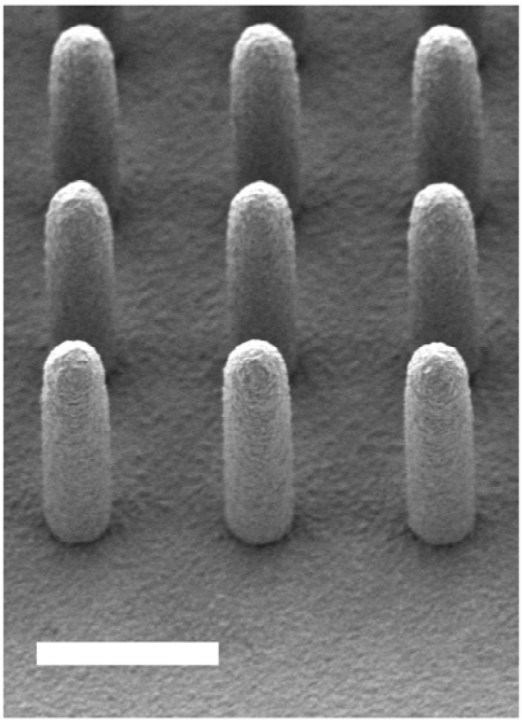

Figure S6. Scanning electron microscope images of a Ni shell in tilt-view from the corner of the array. While a thick layer of Ni was deposited on the wires, there is still no cross deposition between the wires. Scale bar equals 10 μm.

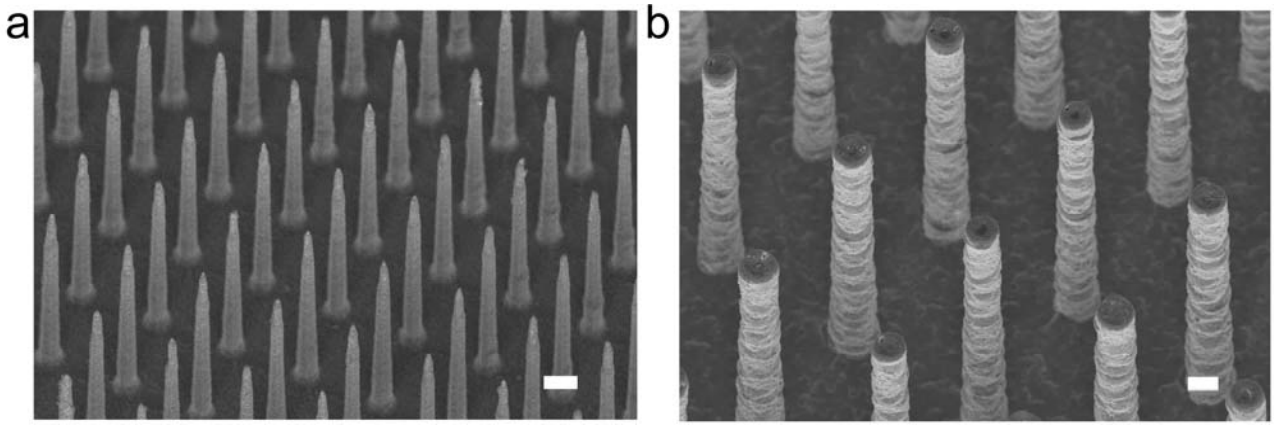

Figure S7. Scanning electron microscope images of (a) polyaniline shell around high conductivity Si wires and (b) polypyrrole shell around low conductivity Si wires are shown. Scale bars equal 2 μm.

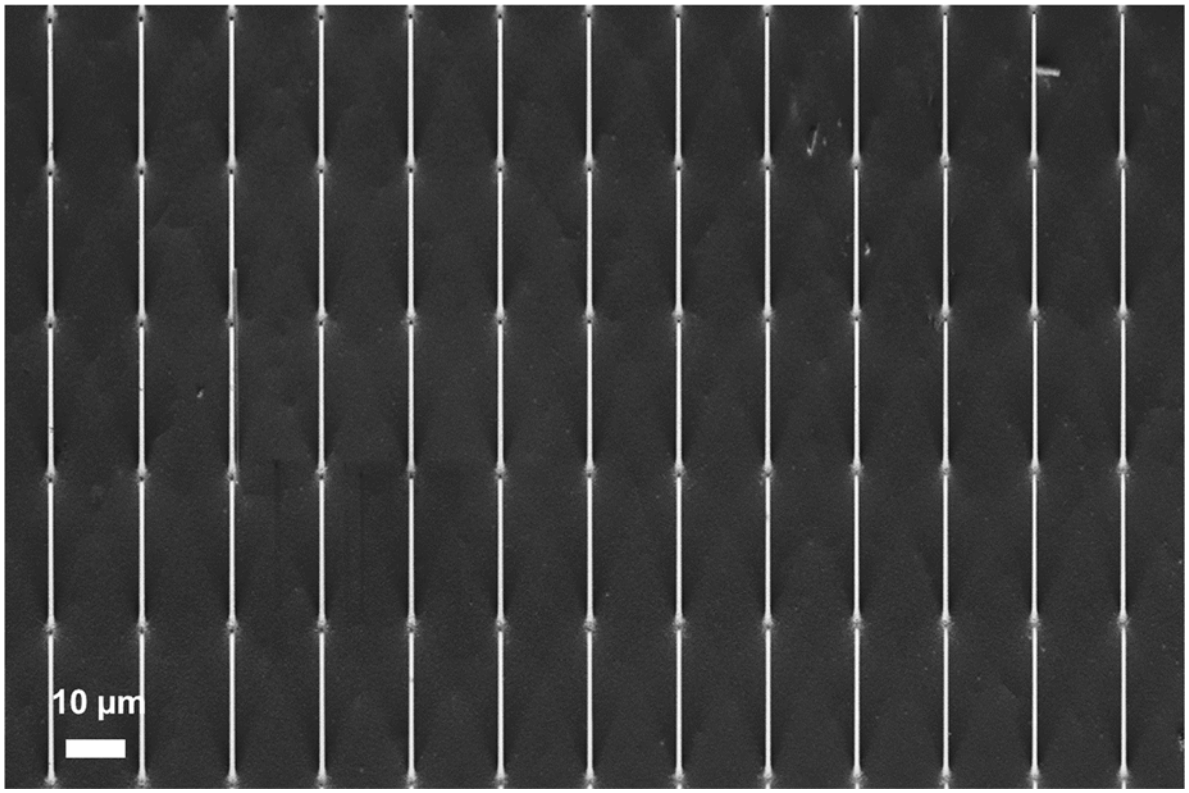

Figure S8. Scanning electron microscope image of Ni-deposited high aspect ratio nanowires.

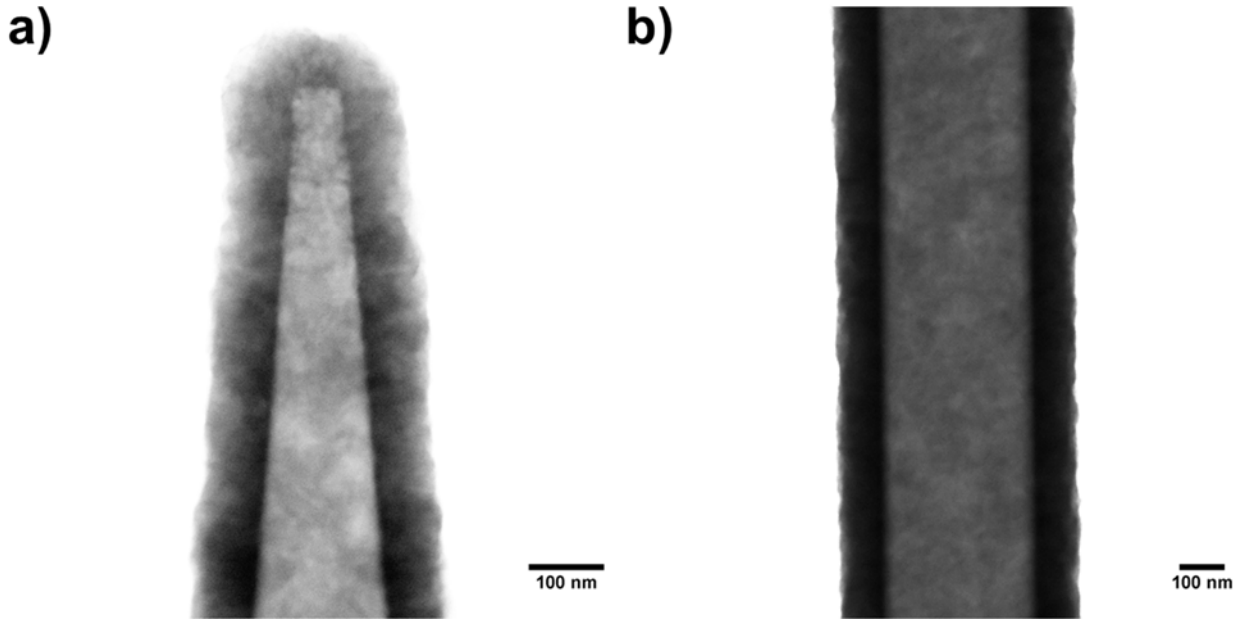

Figure S9. Bright field scanning transmission electron microscope images of the a) tip and b) the body of the Ni-deposited high aspect ratio nanowires.

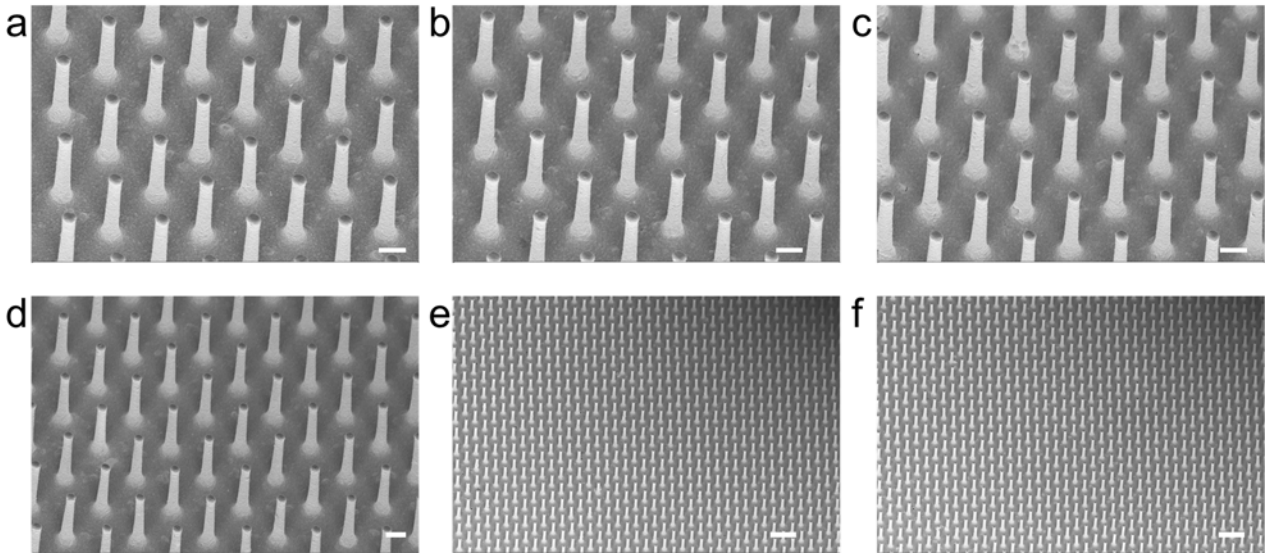

Figure S10. Scanning electron microscope images of Au-deposited silicon wires recorded from different spots on the array at varying magnifications confirming the uniformity of the deposition method on large wire arrays. Scale bar equals 2 μm for a through d, and 10 μm for e and f.

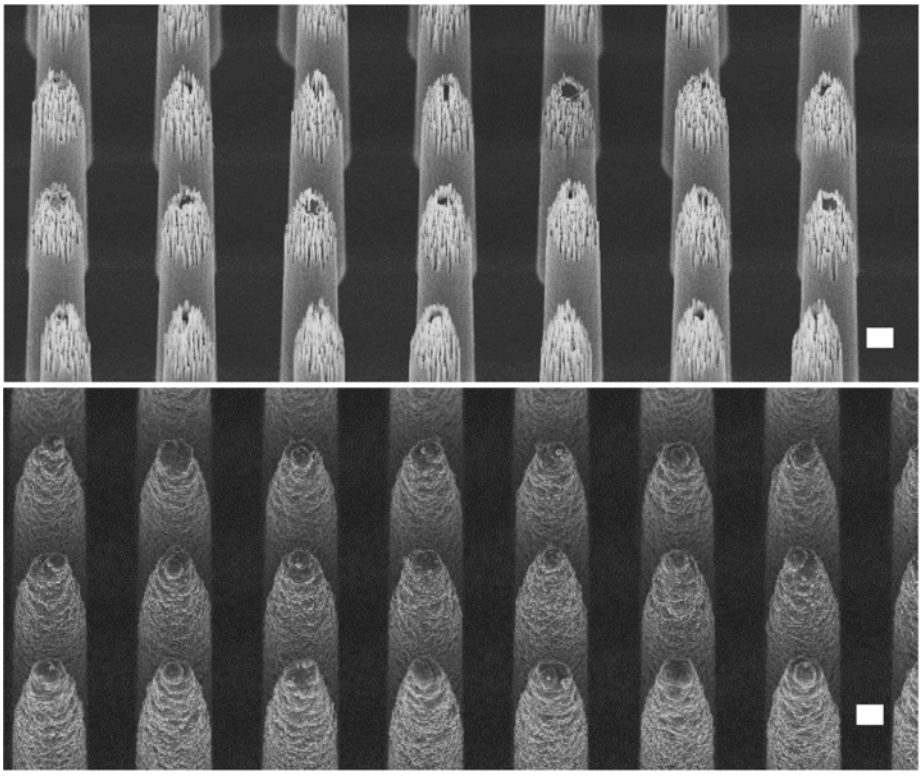

Figure S11. Scanning electron microscope images of before (top) and after (bottom) deposition of a polypyrrole layer on wires with textured tips. Scale bars equal 1 μm.

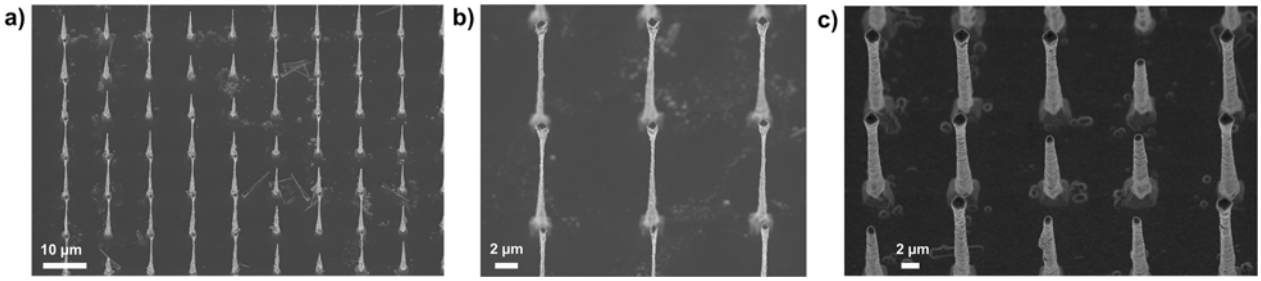

Figure S12. Scanning electron microscope images of hour glass shaped full and broken a) bare silicon wires, b) zoomed in image showing the wire morphology, c) after metal deposition.

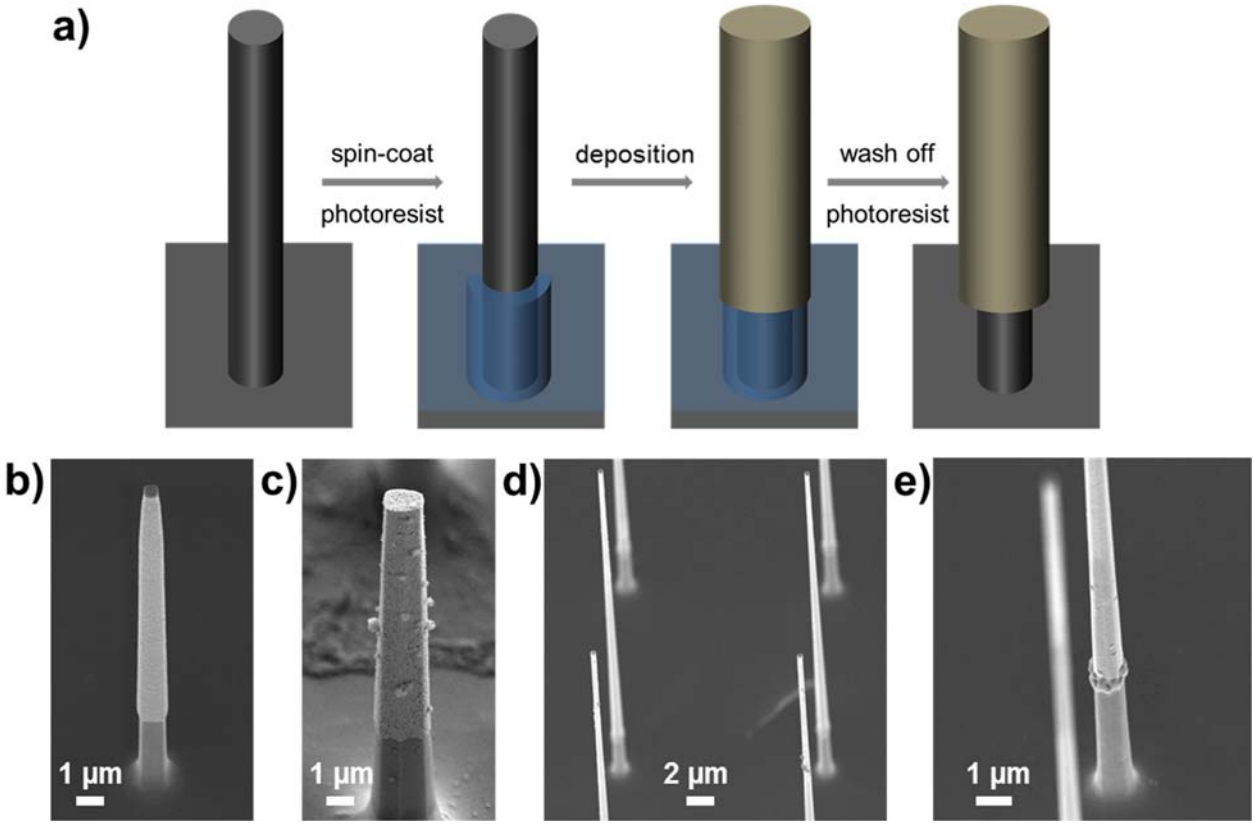

Figure S13. a) Schematic illustration of the masking and electrodeposition process. Scanning electron microscope images of b) Ni and c) Au layered wires after removal of the photoresist matrix. d) and e) high aspect ratio nanowires layered with nickel following a similar approach.

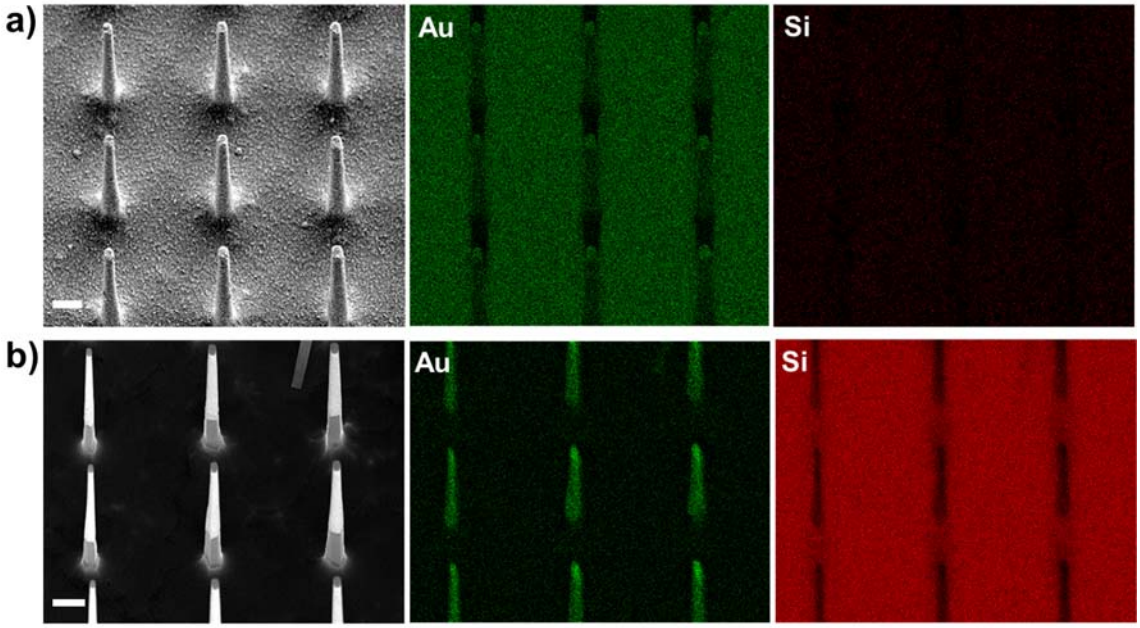

Figure S14. Scanning electron microscope image and elemental maps of Au-deposited silicon nanowire arrays a) without and b) with photoresist masking. Scale bars equal 5 μm.

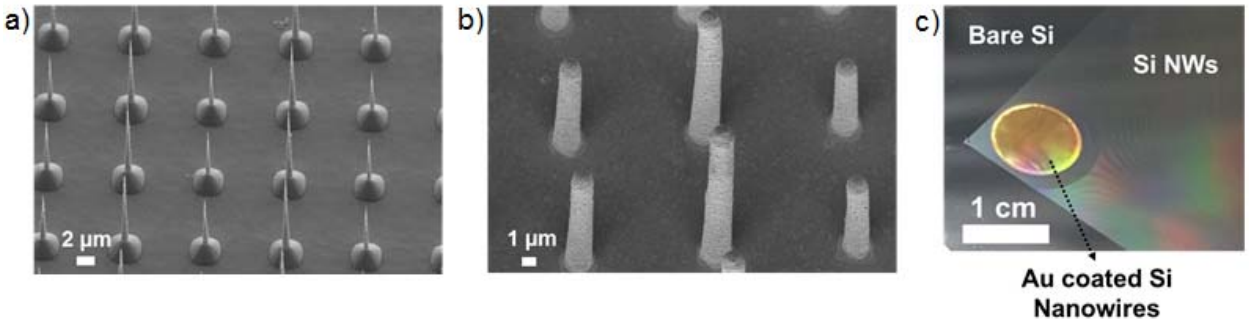

Figure S15. Scanning electron microscope images of short and tall nanowires a) before and b) after Au deposition, and c) photograph of the Au covered wires.

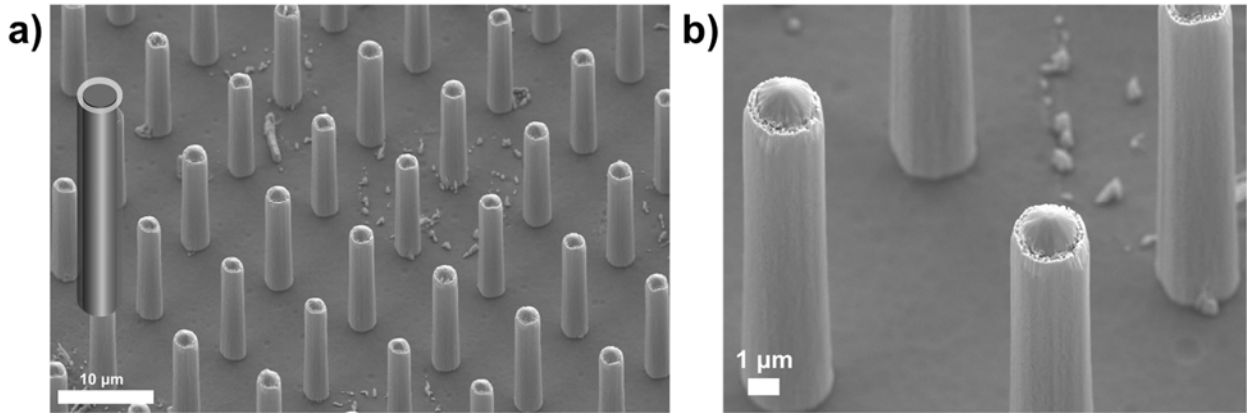

Figure S16. a) Large-view and b) zoomed-in scanning electron microscope images of Ag-deposited nanowires after RIE etching to expose the wire tips.

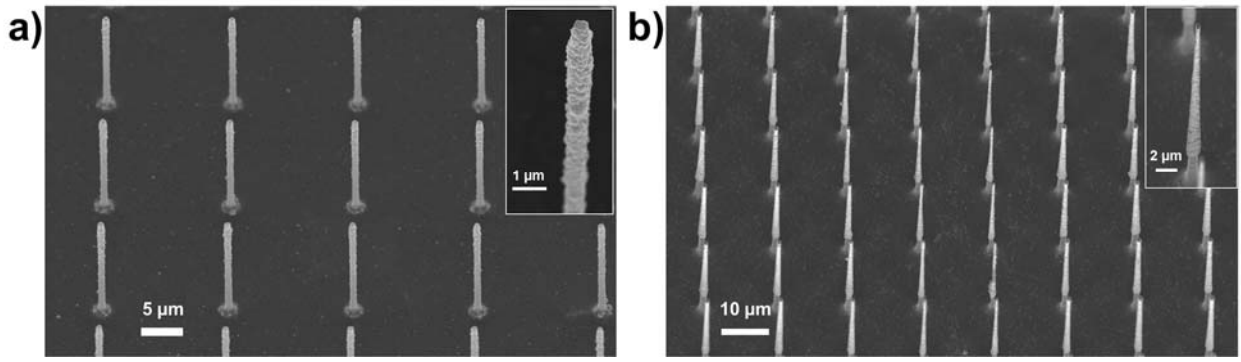

Figure S17. Scanning electron microscope images of a) CdSe deposited nanowires and b) CdS deposited nanowires.

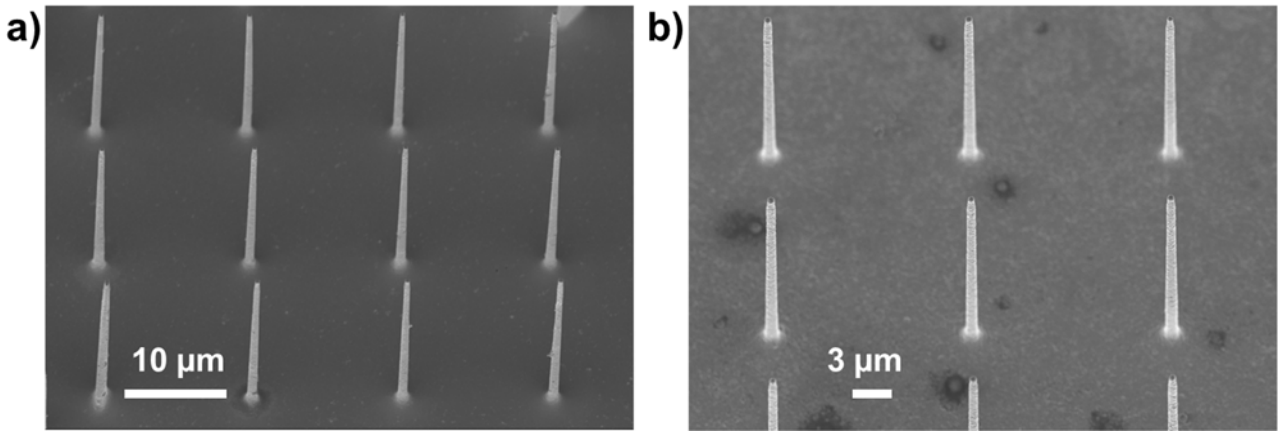

Figure S18. Scanning electron microscope images of a) Rh deposited nanowires and b) Ni-Ru deposited nanowires.

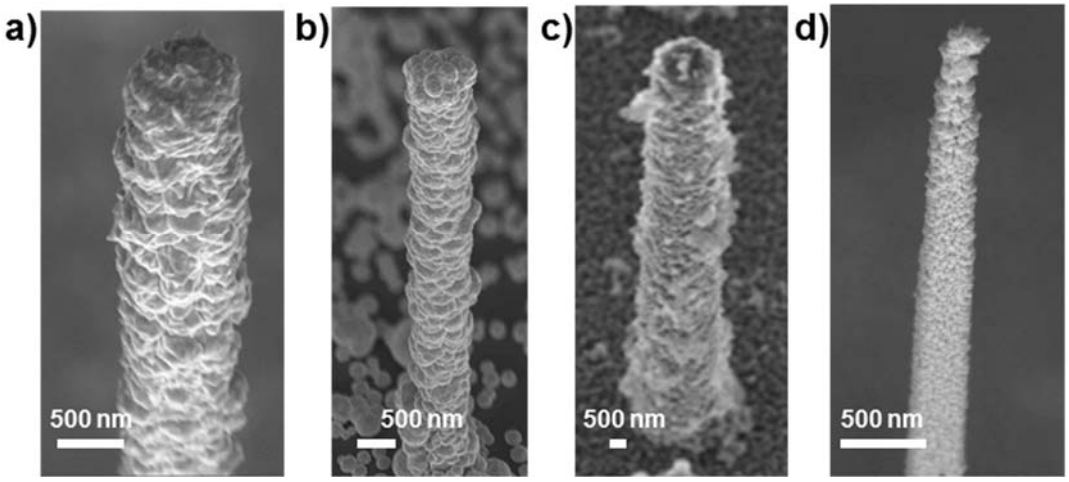

Figure S19. Close-up scanning electron microscope images of a) Cu, b) Pd, c) Fe, and d) Pt deposited silicon wires showing different morphologies based on the material deposited.

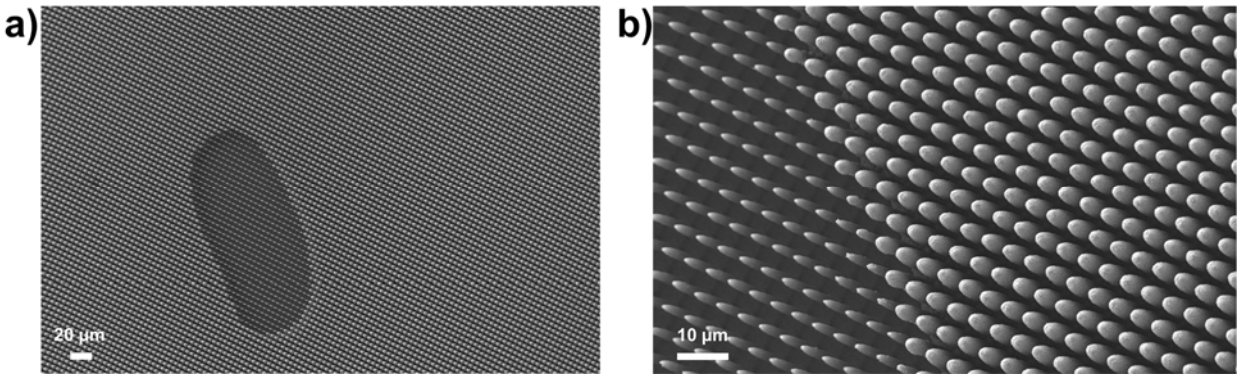

Figure S20. Scanning electron microscope images of a) Ni-deposited nanowires showing an area of bare wires due to a bubble formed on the surface prior to deposition. Zoomed in image in b) shows the detailed difference between the deposited and the unexposed regions.

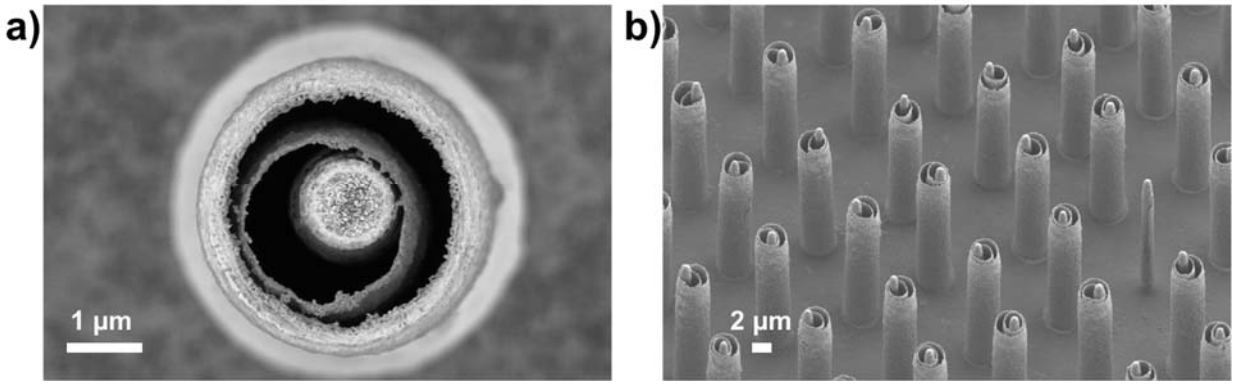

Figure S21. Scanning electron microscope images of very thin coaxial tubes after removal of sacrificial Ni shells. a) Zoomed in and b) large area images show a very thin inner Au shell and a thicker outer Au shell around a silicon wire. Water on the samples were dried without any solvent exchange which caused asymmetric drying of the shells due to capillary forces.