Supporting Information for:

Programmable Resistive-Switch Nanowire Transistor Logic Circuits

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This file includes:

Supplementary Figures S1-S4

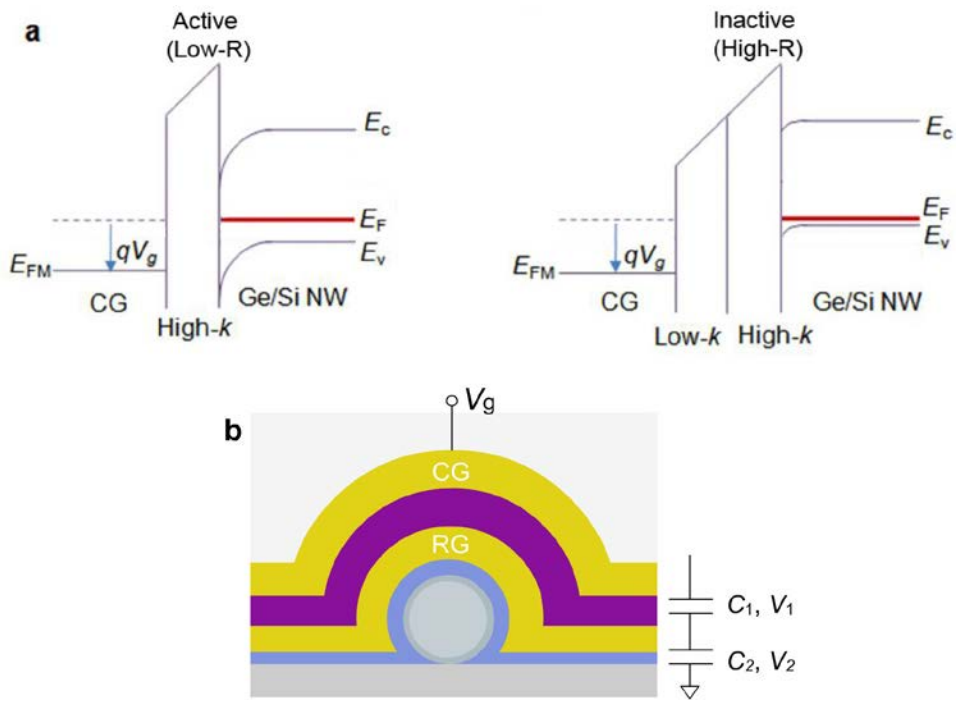


Figure S1. Schematic energy-band diagrams and capacitive coupling of a resistive-switch nanowire transistor at different programmed states. (a) (Left panel) For a programmed active state (the resistive switch is at ON state), the Ge/Si nanowire channel is depleted for a V_g applied on the CG. (Right panel) For a programmed inactive state (the resistive switch is at OFF state), the Fermi level in the Ge/Si nanowire is located in the valence band for the same V_g applied on the CG, yielding a still conducting transistor channel. Here q, E_v, E_F, and E_c denote the electron charge, energies of valence band, Fermi level, and conduction band, respectively. (b) The capacitive coupling in the inactive state with a gate voltage (V_g) applied on CG. The effective voltage on RG (V_2) is reduced to $\frac{C_1}{C_1+C_2}V_g$, where C_1 and C_2 represent the capacitances of CG/SiO_2/RG and RG/ZrO_2/nanowire channel, respectively.

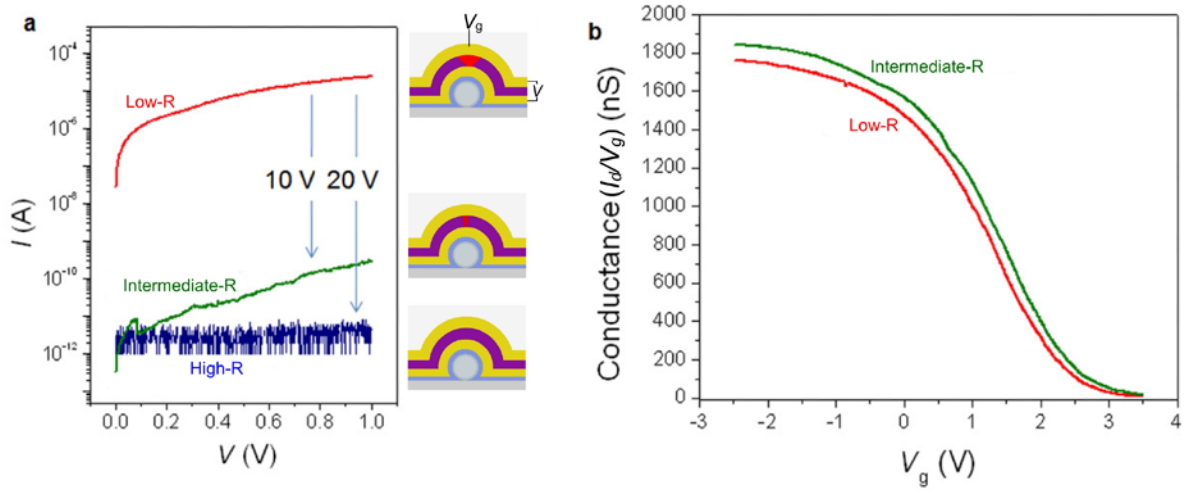


Figure S2. High-R state in the CG/SiO_2/RG resistive switch for capacitive coupling. (a) Intermediate resistance (Intermediate-R) state and High-R state resulted from reset processes using different voltage magnitudes of 10 V (green) and 20 V (blue), respectively, with the corresponding schematics shown in the right panel. (b) CG responses of the transistor channel for the Low-R state (red curve) and Intermediate-R state reset by 10 V (green curve) in the CG/SiO_2/RG. These data show that the intermediate-R state resistance yields dominant resistive (vs. capacitive) coupling, and thereby produces negligible programmable logic window.

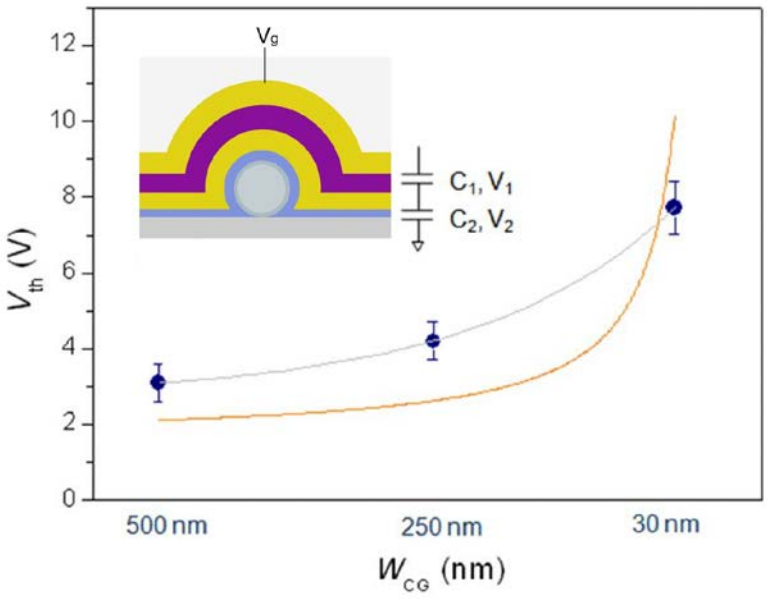
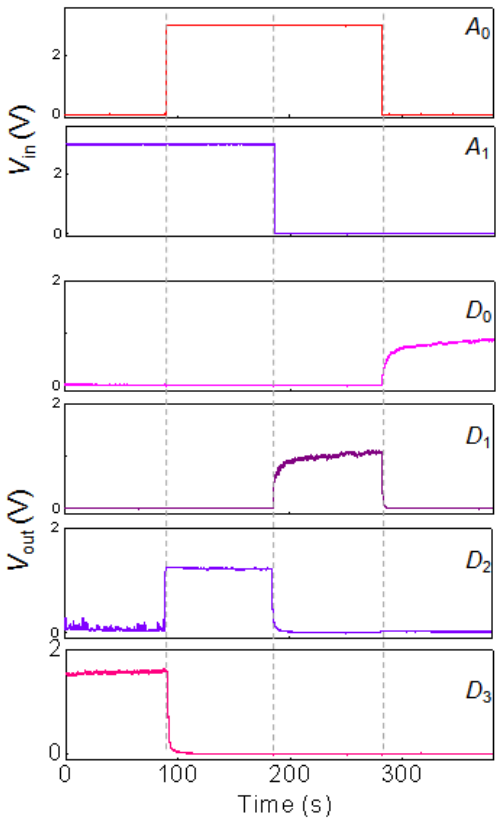


Figure S3. Threshold-voltage (V_{th}) trend with respect to different CG width (W_{CG}) for the inactive state in resistive-swtich nanowire transistor. The blue dots are from the experimental data and the orange curve is calculated trend based on a serial-capacitor model (inset). For the capacitive coupling in the inactive state with a gate voltage (V_g) applied on CG, the effective voltage on RG (V_2) is $\frac{C_1}{C_1+C_2}V_g$, where C_1 and C_2 represent the capacitances of CG/SiO_2/RG and RG/ZrO_2/nanowire channel, respectively. Specifically, $C_1 = \frac{\varepsilon_{SiO_2}(LW_{CG})}{D}$ (planar geometric model) and $C_2 = \frac{2\pi\varepsilon_{ZrO_2}}{\ln\left(\frac{2h+d}{d}\right)}$ (cylindrical geometric model), where ε_{SiO_2}, ε_{ZrO_2}, L, D, h, and d denote the dielectric constants of SiO_2 (3.9 ε_0), ZrO_2 (25 ε_0), overlapped length between CG and RG (7 μm), thicknesses of SiO_2 (30 nm), ZrO_2 (7 nm) and diameter of nanowire (20 nm), respectively. For an empirical V_2 value of ~1.6 V (dashed gray curve in Fig. 2c) to pinch off the Ge/Si nanowire transistor channel, it requires a threshold voltage V_{th} or a minimum $V_g = 1.6 \times \frac{C_1+C_2}{C_1}$.

a



b

A_0	A_1	D_0	D_1	D_2	D_3
0	1	0 (0.02 V)	0 (0.01 V)	0 (0.07 V)	1 (1.55 V)
1	1	0 (0.01 V)	0 (0.01 V)	1 (1.22 V)	0 (0.01 V)
1	0	0 (0.01 V)	1 (1.10 V)	0 (0.01 V)	0 (0.01 V)
0	0	1 (0.89 V)	0 (0.01 V)	0 (0.02 V)	0 (0.01 V)

Figure S4. Retention of the programmed 2-to-4 demultiplexer. (a) Output logic flow from the programmed circuit after 27 days in ambient environment. (b) The corresponding truth table.