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# Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor

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**This file includes:**

## Materials and Methods

**Nanowire nanostructure synthesis.** Single crystal p-doped silicon nanowires (p-SiNWs) were synthesized by the nanocluster-catalyzed vapor-liquid-solid (VLS) process as described previously[1]. Briefly, 100 nm diameter gold nanoparticles (Ted Pella) were dispersed on $SiO_2$/Si growth substrates (Nova Electronic Materials), and growth was carried out at a total pressure of 25 torr, temperature of 450–460 °C, using $SiH_4$ (2.5 sccm), $B_2H_6$ (3 sccm, 100 ppm in He) and Ar carrier (10 sccm) for 20~30 mins. The resulting ca. 100 nm diameter p-SiNWs grown as above were deposited from an isopropanol dispersion onto $Si_3N_4$ surface of silicon wafers (100 nm thermal $SiO_2$, 200 nm $Si_3N_4$, n-type, 0.005 V · cm, Nova Electronic Materials). Germanium nanowire (GeNW) branches, which serve as the template for the final nanotube structures, were also synthesized by the Au nanocluster catalyzed VLS process. A modification of the sequential branch growth process described previously[2] was used (Figs. S1a-c). First, Au nanodots were defined by electron-beam lithography (EBL, JEOL JSM-7000F) and metal evaporation on the top surfaces of the dispersed SiNWs, the chip was placed in the growth reactor, and then GeNW branches were grown using an initial nucleation step at 305-315 °C for 5 min ($GeH_4$ (10 sccm, 10% in $H_2$), $H_2$ (200 sccm), total pressure of 100 torr) and elongation step at 280-295 °C for 20 min (gas flow and pressure same as for nucleation). The GeNW branch diameter, which defines the final $SiO_2$ nanotube inner diameter, is controlled through the size and thickness of the deposited Au nanodots. Growth with Au nanodots of 80 nm diameter and 40 nm thickness yielded average 50 nm GeNW branches on top of SiNW backbones. The GeNW lengths are determined by the growth time with typical values of 2-4 μm. The specific orientation of the GeNWs was not controlled in these studies because the penetration of the nanotubes into cells does not require them to be vertical (see main text). For this reason, we selected and used GeNWs within $30^o$ with respect to the surface normal for BIT-FET devices (see below). We note that alternative methods, such as chemical reduction from solution, can be used to prepare Au particles on SiNWs (without the need for EBL) for GeNW branch growth[2] in a parallel and high-throughput manner.

**BIT-FET device fabrication.** Completion of the nanotube structure and device fabrication were carried out in parallel as shown schematically in Fig. S1. Following GeNW branch growth, resist was coated on the chip (~2 μm copolymer, MMA (8.5) MAA (EL11) and ~0.5 μm PMMA (950

C5), MicroChem Corp.), baked at 180 °C for 10 min. Then EBL and thermal evaporation were used to define Ti/Pd/Ti (1.5/120/10 nm) S/D contacts on each side of selected GeNW branches, which are within 30$^{o}$ with respect to the surface normal, on the corresponding SiNW backbones (Fig. S1d). The typical separation between S/D contacts was 300-700 nm. Critical point drying (Auto Samdri 815 Series A, Tousimis,) was used during lift-off and rinse steps to minimize collapse of the GeNW branches. A uniform layer of $SiO_2$ (~50 nm) was deposited by atomic layer deposition (ALD, Savannah-S200, Cambridge NanoTech) at 250 °C[3], and annealed in the ALD system at 250 °C for 15 min. The conformal $SiO_2$ layer (Fig. S1e) serves both as the nanotube wall (after removal of Ge) and passivation of the metal electrodes. The GeNW core is removed by a sequence of steps shown in Fig. S1 (f-i) to yield the final nanotube device. First, a photoresist protection layer (Shipley S1813 or S1818, MicroChem Corp.) was coated to a thickness smaller than the GeNWs height, baked at 115 °C for 5 min, and then the exposed $SiO_2$ of the GeNW/$SiO_2$ core/shell structure was removed by BHF (Buffered HF Improved, Transene) (20~25 s for ~50 nm ALD $SiO_2$). The BHF etching goes along both the radial and axial direction, which results in a tapered $SiO_2$ shell. Following photoresist lift-off, hydrogen peroxide ($H_2O_2$, 30%, Sigma) was used to selectively etch the Ge (50 ºC, 45-60 min). The final $SiO_2$ nanotube height is defined by the thickness of the photoresist protection layer. Unless specifically mentioned, all devices used in this work, including those for device characterization and cell measurements etc., use nanotube inner diameter and ALD $SiO_2$ thickness of ca. 50 nm, nanotube length of 1-1.5 μm, p-doped SiNWs with diameter of ca. 100 nm.

**Device characterization.** To characterize the response of the BIT–FET devices in aqueous solution, a 2 mm thick polydimethylsiloxane (PDMS) sheet with a 15 mm × 10 mm window was put on the device chip, and the open region was filled with 1× phosphate buffered saline (PBS, Mediatech, Inc.); a Ag/AgCl electrode was inserted into the solution and the FET conductance versus water gate voltage ($V_{wg}$) measurements were carried out by sweeping the voltage while simultaneously recording the FET current with a current preamplifier (1211, DL Instruments). The voltage sweep output/preamplifier output was generated/recorded with a DAC card (PCI-6030E, National Instruments, Inc.) under computer control, with typical ramp speed of 50 mV/s. To assess the temporal response of the BIT-FET devices, a pulsed $V_{wg}$ with variable rise time (0.1-50 ms) was generated (Axon Digidata 1440A Data Acquisition System, Molecular Devices,

Inc.) and the current of the FET was amplified with a home-built current preamplifier, filtered (CyberAmp 380, Molecular Devices, Inc.), and then digitized (Axon Digidata 1440A Data Acquisition System, Molecular Devices, Inc.). Conductance values recorded for BIT-FET devices vary between ca. 1-70 μS. This variation reflects differences in the SiNWs and device configuration, but has no effect on calculated potentials since the sensitivity of each device was determined prior to cell measurements.

**BIT-FET sensitivity**. The sensitivity, which is characterized by the conductance change per unit $V_{wg}$ change (transconductance) is proportional to the gate capacitance[4]. Before GeNW etching (Fig. S3a), the relevant gate capacitance, which reflects the sensitivity of BIT-FET to the solution outside the nanotube, can be estimated[5] with the half cylindrical model (inset, Fig. S3a) as:

$$C_{out} = \pi\varepsilon_0\varepsilon_r L / ln[(d_{SiNW}+2t_{SiO2})/d_{SiNW}] \quad (1)$$

where $\varepsilon_0$, $\varepsilon_r$, $L$, $d_{SiNW}$ and $t_{SiO2}$ are vacuum dielectric constant, relative dielectric constant of $SiO_2$, effective channel length, SiNW diameter and ALD $SiO_2$ thickness,

$$L = L_{app} - d_{base} - 4t_{SiO2} \quad (2)$$

$L_{app}$ is the distance between the two closest edges of S/D electrodes (apparent channel length), $d_{base}$ is the diameter of the GeNW branch base, which is normally larger than the diameter of the GeNW branch body (c.a. 100 nm for 50 nm average diameter GeNW, e.g. Fig. 1b).

After removing the GeNW, solution fills in nanotube and gates the SiNW FET through the thin (1.5 nm, $t_{native}$ as below) native oxide (Fig. S3b). We model the capacitance, $C_{in}$, which reflects the sensitivity of the BIT-FET to solution inside the nanotube, as a parallel plate capacitor[5]:

$$C_{in} = \varepsilon_0\varepsilon_r A / t_{native} \quad (3)$$

where $A$ is the contact area between the SiNW and the solution inside the nanotube. If there is no Ge over-coating, $A$ is equal to the GeNW base area. The transconductance ratio after to before GeNW etching is estimated by the gate capacitance ratio, $(C_{in}+C_{out})/C_{out}$. For the device used in Fig. 2 a-c, this yields a ratio, ~5, which is smaller than the experimental value, ~26.

The enhanced sensitivity difference compared to the idealized calculation is a result of several factors. First, the contact area $A$ can be larger than that defined by the GeNW branch base due to over-coating of Ge on SiNW surface during GeNW growth. Removal of this Ge material over-coated on SiNWs during etching will lead to a longer *active* channel, and larger $A$ and $C_{in}$. We note that SEM images of the BIT-FETs taken after breaking nanotubes at the SiNW-tube junction always show a larger hole than would be defined by GeNW branch base alone, which is consistent with a larger $A$. The upper limit in this context, which corresponds to the entire SiNW surface exposed to the internal solution of the nanotube, would yield a sensitivity ratio of ~50. The experimental ratio falls between these calculated limits, which suggests that the *active* channel exposed to the internal solution of nanotube is smaller than the entire SiNW surface but larger than that defined by the GeNW base. Indeed, device measurements show a range of enhancement ratios and the transconductance/sensitivity values for different BIT-FETs vary for different GeNW growth conditions (different Ge over-coating). We note that because all device sensitivities are characterized, the observed variation does not affect our determination of absolute potential change in the cell measurements. In the future, we anticipate that Ge over-coating could be used to rationally enhance the sensitivity of the BIT-FET devices. Second, the small effective channel length $L$ and relatively thick $SiO_2$ dielectric layer can lead to a reduction in $C_{out}$ due to the screening by the metal S/D electrodes[6]. This would lead to a lower sensitivity than estimated for the BIT-FET prior to GeNW etching.

**Pulsed water gate curve fitting.** In the pulsed $V_{wg}$ measurement, the capacitive coupling current between the passivated metal electrodes (in the open window area) and the solution yield +/- peaks in during the rising/falling edges of the pulse (e.g., Figs. 2d and S4a). To accurately remove these artifacts without affecting the intrinsic BIT-FET signal we carried out the following steps. First, a control device without $SiO_2$ nanotube was fabricated and measured (black trace, Fig. S4a), where the baseline conductance (before and after pulse) and the steady state conductance during the pulse represents the intrinsic SiNW FET response (red trace, Fig. S4a). The +/- peaks obtained by subtracting the intrinsic FET response from the measured data for the control device, yields the pure capacitive coupling signal for the control device. The capacitive coupling signal determined from this analysis for the control device was then scaled by ratio of the exposed electrode areas for the BIT-FET versus control devices, to yield the

capacitive coupling signal of the BIT-FET device, which is then subtracted from the measured data to yield intrinsic device response (red trace, lower panel of Fig. 2d). Note that the subtraction has no fitting parameters and the capacitive coupling artifacts are removed completely.

**Cell recording.** Embryonic chicken cardiomyocytes were cultured using published protocols on thin PDMS films[7,8]. Device chips were incubated with lipid vesicles of 1,2-dimyristoyl-sn-glycero-3-phosphocholine (DMPC, Avanti Polar Lipids Inc.) containing 1% 1-myristoyl-2-{12-[(7-nitro-2-1,3-benzoxadiazol-4-yl) amino] dodecanoyl}-sn-glycero-3-phosphocholine (NBD-lipid, Avanti Polar Lipids Inc.) as fluorescent reporter to form supported lipid layers on devices including nanotube surfaces, using a procedure described earlier[8]. The cell recording measurements were carried out in tyrode solution (pH ~ 7.3) at 30-37°C using a 100 mV DC source voltage for FET devices. The current was amplified with a home-built multi-channel current preamplifier, filtered with a 6 kHz low pass filter (CyberAmp 380), and digitized at 50-250 kHz sampling rate (Axon Digi1440A). Ag/AgCl reference electrodes were used to fix the extracellular solution potential in all recording experiments[7,8]. The PDMS/cell sheets were manipulated using glass micropipettes to control the relative position between the cells and the nanotubes.

**Bandwidth calculation.** The BIT-FET device was modeled by the equivalent circuit shown in Fig. S4b. Resistors $R_1$, …, $R_{i+j}$ are used to model the distributed resistance of the solution inside the nanotube, capacitors $C_1$, …, $C_{i+j}$ model the distributed capacitance between the inside and outside of the nanotube, $R_{access}$ is the access resistance from the solution to the opening of the nanotube, $V_0$ is the intracellular potential of the cell. Outside the cell, the solution outside the nanotube is fixed by the reference electrode, $V_n$ is the potential at the end of the nanotube (SiNW surface), $C_{NW}$ is the gate capacitance of SiNW accessed by the internal solution in nanotube, and $R_{NW}$ is the resistance of the SiNW. The cell electrical potential signal propagates from the opening of the nanotube to its end, where it couples to the FET channel, through the solution. The potential also capacitively couples to the solution outside the nanotube across the $SiO_2$ nanotube wall. Using the Ohm's law and capacitive coupling[5] at any point along the nanotube, the propagation of the electrical potential signal can be described by:

$$\begin{cases} -\dfrac{\partial V_{in}}{\partial z} = \rho_R I \\ -\dfrac{\partial I}{\partial z} = \rho_C \dfrac{\partial (V_{in} - V_{out})}{\partial t} \end{cases} \quad (4)$$

Here $V_{in}$, $V_{out}$, $\rho_R$, $\rho_C$, $I$, $z$, $t$ are potential inside the nanotube, potential outside the nanotube, linear resistivity of solution inside the nanotube (resistance per unit length), capacitance of the nanotube wall per unit length, current, distance from the nanotube opening, and time, respectively. These equations can be rewritten as:

$$\frac{\partial^2 V_{in}}{\partial z^2} = \rho_R \rho_C \left(\frac{\partial V_{in}}{\partial t} - \frac{\partial V_{out}}{\partial t}\right) \quad (5)$$

where $\rho_R$ is calculated from the solution bulk resistivity $\rho_{Bulk}$ by $\rho_R = 4\rho_{Bulk}/\pi d^2$ and $\rho_C$ comes from three parts connected in series: the two electrical double layers on the inner and outer $SiO_2$ surface of the nanotube, and the capacitance across the $SiO_2$ wall. Each part is calculated from the cylindrical capacitor model[5] by $\rho_C = 2\pi\varepsilon\varepsilon_0/ln(a_2/a_1)$, where $\varepsilon$ is the dielectric constant of the material, $a_1$ and $a_2$ is the inner and outer diameter of the cylinder. For example, the capacitance across the $SiO_2$ wall can be written as $\rho_C = 2\pi\varepsilon_r\varepsilon_0/ln\,[(d+2t_{SiO2})/d]$. Here $d$ is the nanotube inner diameter. $\varepsilon_r$, $\varepsilon_0$, and $t_{SiO2}$ are defined as before in the 'BIT-FET sensitivity' part. Overall, the capacitance of the $SiO_2$ wall is the dominant term due tothe large thickness of the $SiO_2$ wall and the relatively small dielectric constant of $SiO_2$ (compared to the water double layer dielectric constant), although we considered all three parts in the calculation.

We evaluate the potential change at the end of the nanotube as a function of time following cell potential change, based on equation (5), using 1-dimensional finite element method (written in Mathematica, Wolfram Research, Inc.). The boundary conditions for the simulation are as follows: Outside the cell, $V_{out}$ is fixed by the reference electrode; inside the cell, $V_{out}$ equals to the intracellular potential of the cell; 1/3 of the nanotube is inside the cell; the gate capacitance, $C_{NW}$, of the SiNW is approximated as a parallel plate capacitor.

The bandwidth is evaluated by using a fast ramp of the cell potential from 0 to the steady-state value $V_0$, and simulating the corresponding change of the potential at the end of the nanotube $V_n$ vs. time. The effective bandwidth, $BW$, is:

$$BW \approx 0.35/\tau \quad (6)$$

where $\tau$ is the time for $V_n$ to change from 10 % to 90 % of $V_0$. For the calculation of the diameter-dependent bandwidth (Fig. 2f), the $SiO_2$ thickness was fixed at the nanotube inner diameter, and the nanotube length was a constant 1.5 μm. The high bandwidth determined for the BIT-FET devices results in large part from the small device capacitances, despite the increasingly large solution resistance within the nanotube with decreasing inner diameter. For example, the resistance of physiological solution inside a 10 nm inner diameter, 1.5 μm long nanotube is ca. 19 GΩ, but the corresponding capacitance is only 0.3 fF.

The above simulation gives the upper limit bandwidth for our BIT-FETs. When the *active* channel extends beyond the area defined by the GeNW base due to the Ge over-coating (see sensitivity discussion above), the bandwidth will decrease. The lower-limit bandwidth for this configuration (red data points, Fig 2f) was calculated using the same finite element method by assuming a 10 nm gap between SiNW and ALD $SiO_2$, and 400 nm *active* SiNW channel length.

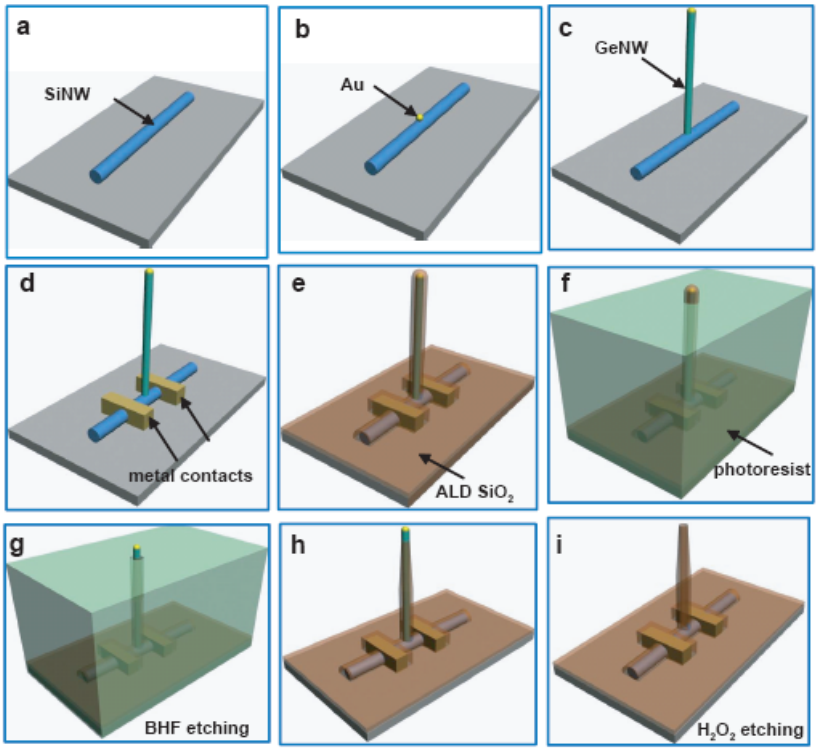


**Figure S1 | Schematic fabrication flow for the BIT-FET device. a**, SiNW is dispersed on substrate. **b**, Au nanodot is defined on the SiNW using EBL and thermal evaporation. **c**, GeNW is grown on top of the SiNW through Au nanodot catalyzed VLS process. **d**, EBL is used to define metal contacts on the SiNW at each side of the GeNW branch. **e**, $SiO_2$ is deposited by ALD to yield a conformal coating over the entire device. **f**, photoresist with thickness smaller than the GeNW branch height is coated on the chip. **g**, BHF is used to etch the $SiO_2$ at the tip of the GeNW branch. **h**, isotropic BHF etching of $SiO_2$ yields tapered nanotube with smaller $SiO_2$ thickness and outer diameter at the upper part of the nanotube. **i**, the GeNW is removed to yield a nanotube connected to the SiNW FET.

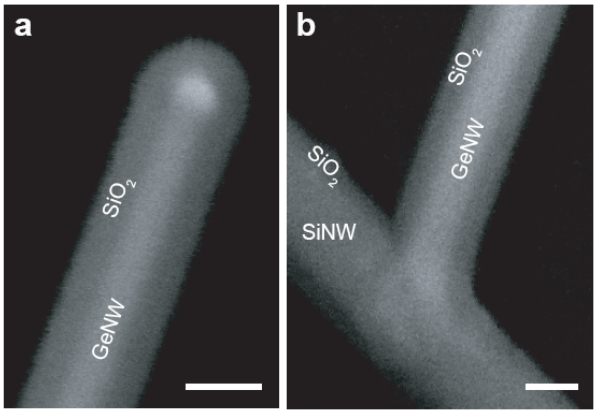


**Figure S2 | High-resolution SEM images of the GeNW/SiNW structure after $SiO_2$ coating. a, b,** top and bottom, respectively, of a GeNW/SiNW structure coated with ca. 50 nm $SiO_2$. scale bars, 100 nm.

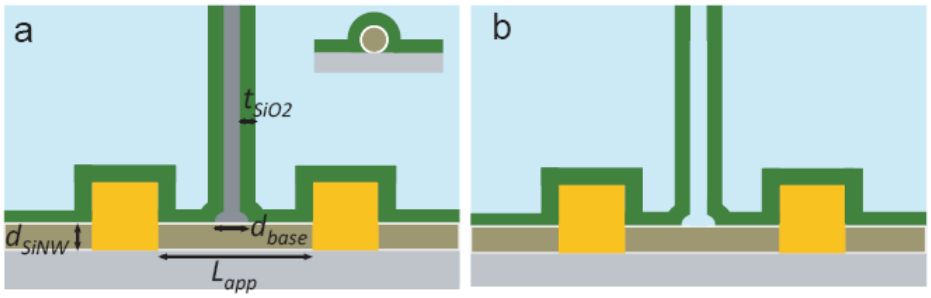


**Figure S3 | Solution access to BIT-FET. a, b,** schematics of the BIT-FET before and after removing the GeNW, respectively. Inset of **a**, the cross-section view of a SiNW coated with conformal ALD $SiO_2$, showing the half cylindrical configuration.

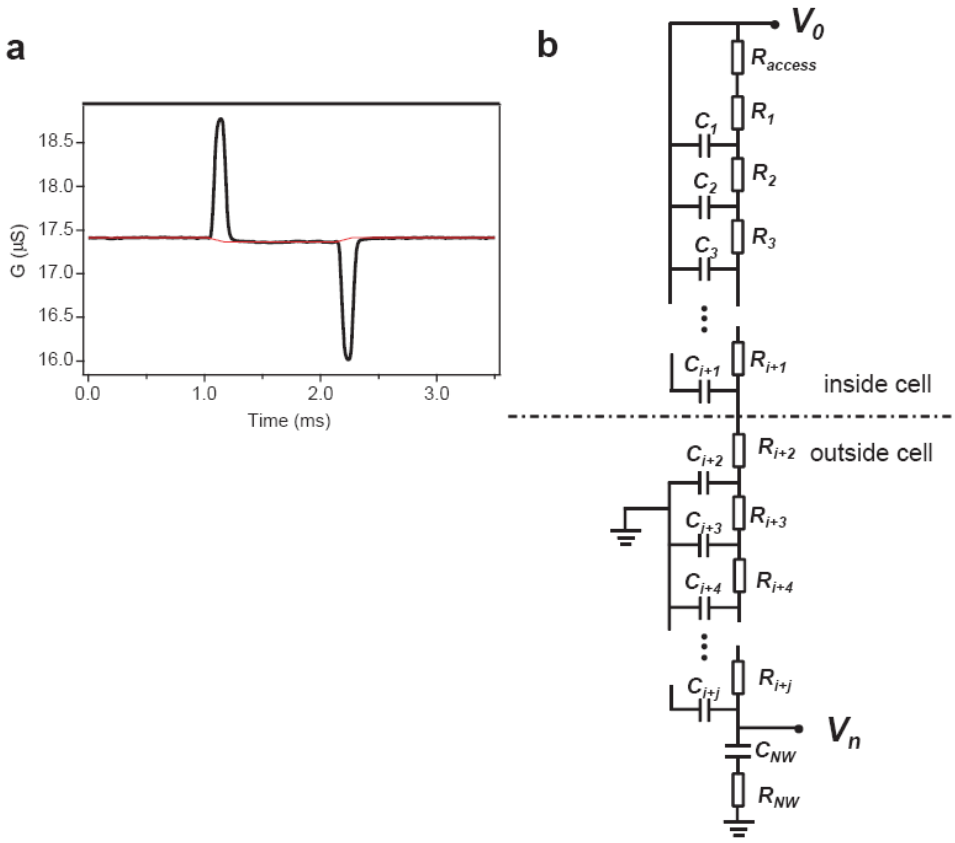


**Figure S4 | BIT-FET device modelling and bandwidth analysis. a**, conductance change versus time for a SiNW FET control device without nanotube (black trace) and the reconstructed intrinsic field-effect response of it (red trace). The $V_{wg}$ pulse used had an amplitude, rise/fall time and duration of 100 mV, 0.1 ms, and 1 ms, respectively. **b**, equivalent circuit for intracellular recording by a BIT-FET device.


**Figure S5 | Robustness of the BIT-FET device.** SEM image of a BIT-FET device after five internalization/retraction cycles with intracellular recording achieved during each cycle. Some residue was observed on the top region of the nanotube at the completion of the multiple internalization/retraction experiment.

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