Nanowire Transistor Performance Limits and Applications

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(Invited Paper)

***Abstract*—Semiconductor nanowires represent unique materials for exploring phenomena at the nanoscale. Developments in nanowire growth have led to the demonstration of a wide range of nanowire materials with precise control of composition, morphology, and electrical properties, and it is believed that this excellent control together with small channel size could yield device performance exceeding that obtained using top–down techniques. Here, we review advances in chemically synthesized semiconductor nanowires as nanoelectronic devices. We first introduce basic nanowire field-effect transistor structures and review results obtained from both p- and n-channel homogeneous composition nanowires. Second, we describe nanowire heterostructures, show that by using nanowire heterostructures, several limiting factors in homogeneous nanowire devices can be mitigated, and demonstrate that nanowire transistor performance can reach the ballistic limit and exceed state-of-the-art planar devices. Third, we discuss basic methods for organization of nanowires necessary for fabricating arrays of device and circuits. Fourth, we introduce the concept of crossbar nanowire circuits, discuss results for both transistor and nonvolatile switch devices, and describe unique approaches for multiplexing/demultiplexing enabled by synthetically coded nanowire. Fifth, we discuss the unique application of thin-film nanowire transistor arrays on low-cost substrates and illustrate this with results for relatively high-frequency ring oscillators and completely transparent device arrays. Finally, we describe 3-D heterogeneous integration that is uniquely enabled by multifunctional nanowires within a bottom–up approach.**

***Index Terms*—Flexible and transparent electronics, heterogeneous integration, high-performance transistor scaling, nanoelectronics, nanowire, 1-D heterostructure.**

I. Introduction

NANOWIRE field-effect transistors (NWFETs) have been proposed and now studied by many research groups around the world as a promising candidate to sustain the relentless progress in scaling for CMOS devices (or MOSFETs) [1]. Several key factors have contributed to the boom of nanowire research. First, semiconductor nanowires can be prepared in high-yield with reproducible electronic properties as required for large-scale integrated systems [2]–[4]. Second, compared with "top–down" nanofabricated device structures, "bottom–up" synthesized nanowire materials offer well-controlled size in at least one critical device dimension, channel width, that is at or beyond the limits of lithography. In addition, the crystalline structure, smooth surfaces and the ability to produce radial and axial nanowire heterostructures can reduce scattering and result in higher carrier mobility compared with nanofabricated samples with similar size [5], [6]. Finally, since the body thickness (diameter) of nanowires can be controlled down to well below 10 nm [7], the electrical integrity of nanowire-based electronics can be maintained even as the gate length is aggressively scaled, a feat that has become increasingly difficult to achieve in conventional MOSFETs.

The electrostatics of NWFETs can be discussed in analogy to fully depleted silicon-on-insulator (SOI) MOSFETs. The surface potential Φ_f in the FET channel is described by a 1-D modified Poisson equation in the following form [8], [9]:

$$\frac{\partial^2 \Phi_f(x)}{\partial x^2} - \frac{\Phi_f(x) - \Phi_{\rm gs} - \Phi_{\rm bi}}{\lambda^2} = -\frac{e\rho(x)}{\varepsilon_{\rm Si}}. \quad (1)$$

Here, $\Phi_{\rm gs}$ and $\Phi_{\rm bi}$ are the gate and built-in potentials, respectively, ρ is the carrier density, $\varepsilon_{\rm Si}$ is the silicon dielectric constant, and the channel is in the x-direction. $\lambda = \sqrt{(\varepsilon_{\rm Si}/\varepsilon_{\rm ox})t_{\rm Si}t_{\rm ox}}$ is termed the natural length [9] and provides a measure of how effectively the gate potential $\Phi_{\rm gs}$ modulates the surface potential Φ_f; $t_{\rm ox}$ and $t_{\rm Si}$ are the gate oxide and channel layer (body) thicknesses, respectively. In the case that the gate length L is larger than five to ten times λ, the second term in (1) dominates, thus minimizing the short-channel effects (SCEs). As a result, to maintain good electrostatic integrity and suppress the SCE, λ must be scaled along with the gate length by reducing $t_{\rm Si}$, $t_{\rm ox}$, and/or increasing $\varepsilon_{\rm ox}$ through the introduction of high-κ dielectrics. In the case of NWFETs, $t_{\rm Si}$ is the diameter of the nanowire and can readily be reduced to a few nanometers—a size scale that is challenging to obtain using conventional lithography means. Furthermore, free-standing nanowire structures enable straightforward implementation of gate structures in semicylindrical or full-cylindrical (Fig. 1)

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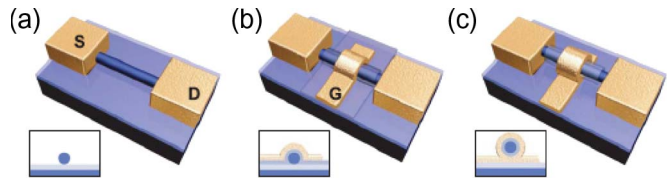

Fig. 1. Schematic of NWFETS with (a) back gate, (b) semicylindrical top gate, and (c) cylindrical gate-all-around configurations. The nanowire is dark blue, gate-dielectric is light purple, and source (S), drain (D), and top-gate (G) electrodes are gold. Insets show device cross section at midpoint between source and drain.

geometries that can lead to a further decrease of λ [8], [9] and, thus, reduce the SCE and improve the drive current as desirable for high-performance operation.

The most well-established method to produce nanowires employs nanocluster catalyzed vapor–liquid–solid (VLS) growth process [3], [4] in which a nanocluster is used to define nucleation and subsequent nanowire growth. The vapor phase source material can be provided in a chemical vapor deposition (CVD), chemical beam epitaxy (CBE), laser ablation, or thermal evaporation reactor. Nanowire growth mechanisms have been elaborated in several recent reviews [2], [3] and will not be discussed in detail here. We want to emphasize that the nanocluster-catalyzed VLS growth approach [2], [3], particularly for CVD or CBE processes, offers the ability to fine tune the diameter, morphology, and, critically, the electrical properties of the nanowires in a flexible and controllable fashion. For example, modulation doping can be achieved by adjusting the dopant concentration *in situ* during nanowire growth [10]. Radial and axial nanowire heterostructures that offer intriguing electrical properties can be produced by switching on and off different source materials during the VLS growth process [11]. The ability to control nanowire growth down to the atomic level is one of the main factors leading to the great success that nanowire research enjoys today.

II. Homogeneous Nanowire-Based Devices

In the case of nanowires with homogeneous structure and composition, silicon nanowires (SiNWs) have most extensively been studied [12]. This is due partly to the dominance of Si in the semiconductor industry, but also reflects the high-level of control of structure and doping demonstrated in fundamental SiNW growth studies [12], [13]. In addition, other nanowire materials such as Ge, InAs, GaN, and metal oxides have also received broad attention [14]–[17].

A. SiNWs, Early Days

Research on nanowires began to accelerate in 1998, when SiNWs with diameters < 20 nm and lengths > 1 μm were demonstrated using a laser-ablation method [4], [18]. A key concept introduced in this paper was that nanoscale clusters could be used to nucleate and direct the growth of nanowires, in contrast to previous VLS studies of silicon whiskers [19], [20] where a lower limit was presumed to be on the order of 0.1 μm due to equilibrium thermodynamic constraints on the liquid droplet sizes. The ability to prepare nanowires with diameters < 20 nm made it possible for the first time to produce devices that could approach a 1-D limit desirable for high-performance FETs. Initial efforts led to demonstration of NWFETs and basic devices configured using a crossed-nanowire geometry, including p-n diodes and bipolar transistors [21]–[23]. However, the electrical properties of nanowires in these initial studies were far from optimal, for example, leading to low apparent carrier mobilities and large sample to sample variations. These studies thus underscored the importance of growth of nanowires with controlled material and electrical properties.

B. CVD Growth of SiNWs

The development of CVD-based nanowire growth has led to much better control over the doping level and electrical properties of SiNWs and, correspondingly, the realization of high-performance p- and n-channel SiNW FETs, as shown in Fig. 2 [12], [24]. In the most commonly used device geometry, a SiNW is deposited on a SiO_2/degenerately doped-Si substrate with the Si substrate serving as the back gate. Metal electrodes are fabricated through e-beam or photolithography and serve as the source and drain electrodes that complete the FET structure [12] [Fig. 1(a)]. The improved control of doping during growth ensures achieving the desired doping level and uniform device performance. However, the use of metal S/D contacts suggests that such NWFETs are effectively Schottky barrier devices [25]–[27], in contrast to conventional MOSFETs having degenerately doped semiconductor source/drain contacts. Typically, positive Schottky barriers are observed at the metal/semiconductor interface due to the combined effect of metal work function and Fermi level pinning by surface states [28]. As a result, the device performance is to a large degree affected by contact properties [26], [27]. For example, annealing can lead to the formation of effectively ohmic contacts and dramatically increase the on-current and the apparent field-effect mobility $\mu_{\rm fe}$ [12]. In a study on boron-doped Si nanowires, it was found that the I–$V_{\rm ds}$ curves became more linear and symmetric at low bias, and the transport behavior became more stable after annealing, with the measured conductance increasing by threefold. In addition, the two-probe resistance decreased 260 fold from $>$ 100 to 0.62 MΩ, and the measured field-effect mobility $\mu_{\rm fe}$ increased from 30 to 560 cm^2/V $\cdot$ s [12].

The mobility of nanowire devices can be extracted from the measured transconductance $g_m = dI/dV_g$ using the following equation for a long-channel FET at low $V_{\rm ds}$ [28]:

$$g_m = \frac{\mu C}{L^2} V_{\rm ds} \tag{2}$$

where C is the total gate capacitance and L is the gate length of the device. On the other hand, the measured transconductance $g_{\rm ex}$ including the effects of finite source/drain contact resistances is reduced from its intrinsic value $g_{\rm in}$ to [29]

$$g_{\rm ex} = \frac{g_{\rm in}}{1 + g_{\rm in} R_s + (R_s + R_d)/R_{\rm in}} \tag{3}$$

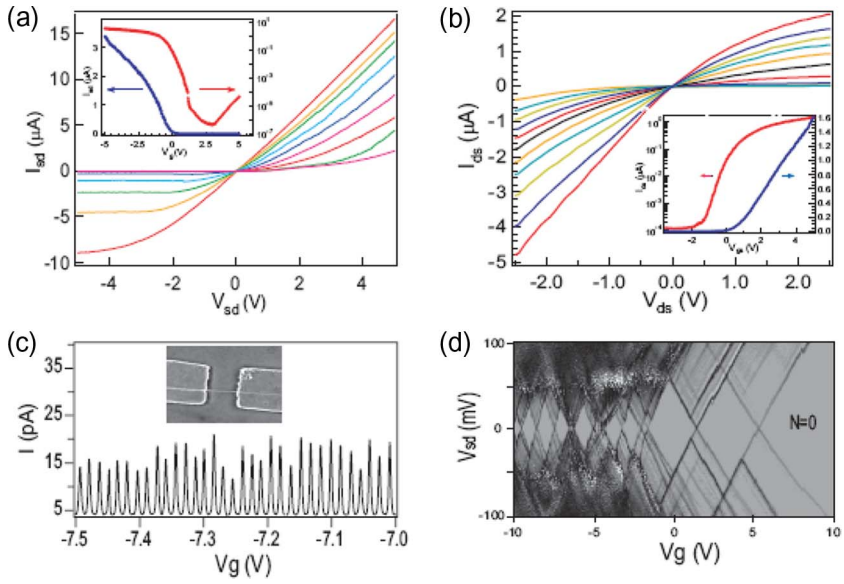

Fig. 2. (a)–(b) Transistor characteristics of p- and n-type nanowires. Insets show transfer characteristics of the back-gated devices. (c) CB oscillations observed at 4.2 K in molecular-scale diameter SiNW; inset shows SEM image of the $L \sim 400$ nm device. (d) $\partial I/\partial V_{\rm sd} - V_{\rm sd} - V_g$ for a $L \sim 50$ nm device at 4.2 K, where carriers are completely depleted ($N = 0$) for $V_g > 5.5$ V. Adapted from [13], [31], and [27].

where R_s and R_d are the source and drain contact resistance, respectively, and $R_{\rm in}$ is the intrinsic resistance of the nanowire channel. It is clear form (3) that contact resistances can greatly influence the performance of NWFETs. For example, in the extreme case when $R_s \gg 1/g_{\rm in}$, the apparent transconductance $g_{\rm ex} \sim 1/R_s$ and can no longer be improved through improvements in $g_{\rm in}$.

This contact resistance effect has been observed in both p- and n-type SiNWs [12], [13]. For example, when phosphorous doping was increased from Si:P growth ratios of 4000 : 1 to 500 : 1, the transconductance was found to increase although the electron mobility is expected to decrease at higher doping levels [13], [28]. This discrepancy can be explained by the fact that Ohmiclike contacts with lower R_s were obtained with heavily doped nanowires compared with those with lightly doped nanowires. Indeed, four-probe measurements show that contact resistances to the lightly doped nanowires can be comparable to the nanowire resistance $R_{\rm wire}$ itself, while those to heavily doped nanowires are negligible compared to $R_{\rm wire}$. After correction of the contact resistance effects the estimated intrinsic mobility was found to decrease from 260 to 95 $\rm cm^2/V \cdot s$ as the doping level increases, in good agreement with values reported for bulk Si [30] assuming the doping concentration is determined by the reactant ratio used to synthesize the nanowires. These results and analysis highlight the important and often underappreciated role that contacts can play in determining NWFET carrier mobility.

The Schottky barriers at the contacts may function as tunnel barriers, and have allowed the properties of SiNW devices to be further analyzed at low temperatures. In particular, studies have demonstrated Coulomb blockade (CB) and coherent charge transport in SiNWs with diameters down to 3–6 nm and source–drain separations ranging from 100 to 400 nm [Fig. 2(c) and (d)] [27]. Fig. 2(c) shows periodic I–$V_{\rm gs}$ oscillations confirming that the device essentially acts as a single quantum dot with each current peak corresponding to the addition of an elemental charge [27], [32]. The measured gate capacitance C_g from the CB oscillations was found to scale linearly with source–drain separation and agrees well with that calculated for the device geometry. These results showed that the quantum dot is formed by the entire length of nanowire between S/D contacts. Coherent charge transport through discrete quantum states was further verified from transport and temperature dependence measurements on devices with diameters down to 3 nm and S/D spacing of 100 nm. In addition, coherent charge transport through a single quantum dot is maintained until the last charge (hole) is depleted [Fig. 2(d)]. These observations are in stark contrast with Si nanowires fabricated by top–down lithography approaches, in which low-temperature studies have typically revealed serially connected quantum dots arising from variations in the channel potential due to structural and/or dopant fluctuations [33], [34] and, thus, corroborate with the high-performance observed at room temperature for the bottom–up nanowire transistors.

C. Germanium Nanowires (GeNWs)

GeNW FET devices have also been studied by several groups [14], [35], [36] due to the higher electron and hole mobilities compared with Si [28]. GeNWs have been synthesized using the nanocluster-catalyzed VLS approach in a CVD process at a relatively low temperature of $\sim$275 °C [14], although an initial nucleation step at 320 °C was found to greatly improve the nanowire yield [35]. Compared to SiNW FETs, GeNW devices are expected to have smaller contact effects because the smaller Ge bandgap will yield a lower Schottky barrier at the metal/NW interface. For example, studies of p-type GeNW devices with Pd S/D contacts yielded a hole mobility of 600 $\rm cm^2/V \cdot s$ [14]. In addition, complementary n- and p-type GeNW devices were demonstrated based on a surface doping approach to prevent uncontrolled sidewall deposition during the nanowire growth [35]. Prototype

gate-all-around devices were also demonstrated by Zhang *et al.* [36] using atomic-layer deposition and magnetron sputtering to uniformly coat an Al_2O_3 dielectric layer and an Al gate layer. Compared with the back-gated GeNW devices, the gate-all-around devices showed excellent subthreshold performance and SCE control due to the improved electrostatics. The ON-state performance of these latter devices was lower than earlier studies due to the series resistance caused by the finite positive (albeit small) Schottky barriers.

D. InAs Nanowires

InAs nanowires have widely been studied as a building block for n-type FETs [37]–[41]. InAs is an attractive material for several reasons. First, its small effective electron mass $(0.023\ m_0)$ results in high electron mobility in bulk materials. Second, an electron gas layer is known to form at the surface of planar InAs due to Fermi level pinning in the conduction band at the surface. Third, the formation of an electron gas combined with the small band gap (0.35 eV) should relatively yield transparent contacts to InAs nanowire devices.

InAs nanowires can be grown using the nanocluster catalyzed process in which the reactant species are delivered by CBE [37], [38] or metal–organic CVD [39]. Studies of InAs NW FETs have yielded depletion-mode n-channel FETs with electron mobilities on the order 3000 $cm^2/V \cdot s$ [39], [40]. The epitaxial growth of InAs nanowires have led to the demonstration of vertical nanowire structures with a wrap-around gate with a low saturation voltage of 0.15 V [41], a topic that will be discussed in detail in Section IV. In addition, the clean electron conduction channel has led to the demonstration of quantum devices including single-electron transistors and quantum dots in CBE grown InAs/InP nanowire axial heterostructures in which the InP layers serve as tunnel barriers [40].

E. Metal Oxide Nanowires

Another class of nanowires that have widely been studied are metal oxides including ZnO, SnO_2 and In_2O_3. A number of methods, including thermal evaporation/vapor transport [42], [43], hydrothermal [44], metal–organic CVD [45], [46], pulsed laser deposition [47], and molecular-beam epitaxy [48] have been used to grow metal-oxide wires while thermal evaporation/vapor transport deposition being the most popular choice due to its low equipment and operation cost [49]. For example, controlled Sb doping during SnO_2 nanowire growth can tune the nanowire's electric properties from nearly intrinsic to metallic (degenerately doped) [50]. Lightly doped SnO_2 nanowires were found to be sensitive gas and UV sensors, while moderately doped SnO_2 nanowires can be made into transparent transistor devices with mobility values up to 550 $cm^2/V \cdot s$ [50]. On the other hand, degenerately doped SnO_2 and In_2O_3 nanowires exhibit metallic properties with resistivities $< 10^{-4}\ \Omega \cdot cm$ [51], [52]. Such nanowires have been studied in applications ranging from optoelectronics devices [53]–[55], field-effect transistors [56]–[58], ultrasensitive nanoscale gas sensors [59]–[62], and field emitters [63], [64].

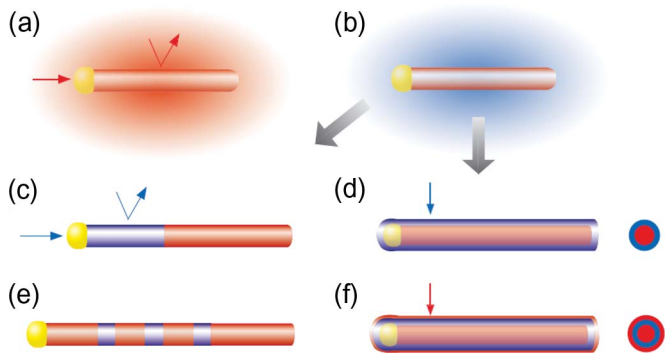

Fig. 3. Nanowire heterostructure growth. (a) Preferential reactant incorporation at the nanocluster catalyst leads to 1-D axial growth. (b) Change in the reactant leads to either (c) axial heterostructure growth or (d) radial heterostructure growth depending on whether the reactant is preferentially incorporated (c) at the catalyst or (d) uniformly on the nanowire surface. Alternating reactants will produce (e) axial superlattices or (f) core-multishell structures. Adapted from [69].

III. Heterostructure Devices

The room temperature and low-temperature measurements discussed above showed that metal S/D contacts yield Schottky-barrier-type contacts in most homogenous nanowire devices. Annealing can improve the contacts and lead to apparent ohmic behavior, for example through the formation of NiSi/Si contacts [65], although this method is still most effective for heavily doped materials. Integrating heavily doped semiconductor S/D contacts with lightly doped nanowire channels (i.e., MOSFET-type devices) has remained challenging, although progress has recently been made using both postgrowth treatment [66] and *in situ* doping methods [10]. On the other hand, transparent ohmic contacts with low contact resistance to lightly doped or intrinsic channel may be achieved in heterostructure nanowire devices through band-structure engineering, making it possible to probe the ultimate performance of the nanowire-based electronics.

A. Heterostructure Nanowire Growth

Perhaps one of the most unique aspects that set the "bottom–up" nanowire system apart is the ability to obtain nanowire heterostructures in a controlled fashion during growth, including radial core/shell heterostructures and axial superlattice heterostructures that are very challenging to match or achieve by lithographic means. The growth of axial and radial nanowire heterostructures are schematically shown in Fig. 3 [11], [37], [67]–[69]. To understand the rational formation of nanowire heterostructures within the context of the VLS method, consider the possible effects of changes in reactant vapor once nanowire growth has been established (Fig. 3). If vapor decomposition/adsorption exclusively continues at the surface of the catalyst nanocluster site, crystalline growth of the new semiconductor will continue along the axial direction [Fig. 3(c)] and repeated changes of reactants in this regime will lead to the formation of an axial nanowire superlattice [Fig. 3(e)] [11], [37]. On the other hand, if the reactant decomposition is favored on the surface of the semiconductor

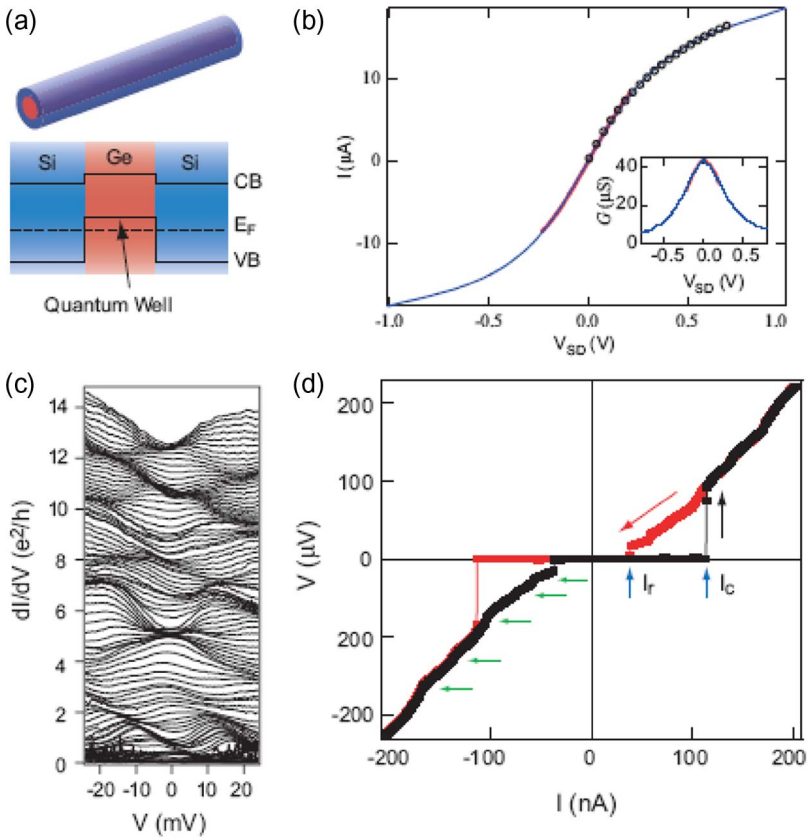

Fig. 4. (a) Schematics of a cross section through the Ge/Si core/shell structure and band diagram. The dashed line indicates the position of the Fermi level, E_F, which lies inside the Si band gap and below the Ge valance band edge. (b) Similar transport characteristics of a Ge/Si core/shell nanowire device measured by (red) four-probe and (blue) two-probe techniques; circles are a fit using a model incorporating LO phonon scattering at high bias. (c) $(dI/dV) - V$ plots recorded at $V_g = 0.8$ to -3.5 V from bottom up in 50-mV steps with no offset applied ($T = 10$ K). (d) Four-probe V–I data measured for a Ge/Si nanowire with Al contacts at $V_g = -3.5$ V and 60 mK. Black and red curves correspond to different current sweeping directions as indicated by arrows. The horizontal green arrows point to the kink structures due to multiple Andreev reflections. Blue vertical arrows point to the positions of the critical current, I_c and the return current, I_r. Adapted from [5], [6], and [77].

nanowire a shell of material will grow on the original nanowire surface [Fig. 3(d)] and changing reactants in this radial-growth regime will result in core-multishell radial structures, as shown in Fig. 3(f) [67]. It is important to mention that there are few constraints on the composition of the shell growth: Any material suitable for planar film deposition can be deposited on the surface of a nanowire, and crystalline radial heteroepitaxy can routinely be achieved [67]. Axial nanowire heterostructures have led to the demonstration of single-electron transistors [68] and optical barcodes [11], [37]. In the following, we will focus on high-performance electrical devices based on radial nanowire heterostructures.

B. Ge/Si Core/Shell Heterostructure Nanowires

One technically important nanowire heterostructure is the Ge/Si core/shell system [5], [6], in which a typically 3–5 nm Si shell is epitaxially grown on top of a ~10-nm-diameter Ge nanowire core. Due to the large, ~0.5-eV valence band offset between Ge and Si, the Fermi level, pinned inside the Si bandgap, is below the Ge valence band [Fig. 4(a)]. This band line-up results in a negative Schottky barrier (i.e., Ohmic contact) to the Ge channel and favors electrical injection of holes to the Ge core from the contacts. As a result, a hole gas is formed and confined inside the Ge core even when intrinsic core and shell materials are used [5]. There are two key advantages of the Ge/Si core/shell heterostructure compared with homogeneous Si or Ge nanowires: First, the formation of transparent (negative Schottky) contacts to the conduction channel and, second, the elimination of dopant scattering. These two factors have led to the successful demonstration of ultrahigh performance transistor devices based on the Ge/Si system [5], [6], [70].

1) Transport Studies: Detailed transport studies have been carried out to examine the Ge/Si nanowire system [5]. As shown in Fig. 4(b), contacts to the hole gas remain transparent even at low temperatures and when the device is close to fully depleted, verifying the band line-up in Fig. 4(a). At 4.7 K, a conductance plateau was observed in the $dI/dV_{\rm ds} - V_{\rm gs}$ curve at a $dI/dV_{\rm ds}$ value close to $2e^2/h$, consistent with predictions for ballistic transport through a 1-D conductor with a single occupied 1-D subband [71]. Furthermore, the basic shape of the $dI/dV_{\rm ds} - V_{\rm gs}$ curve was preserved up to room temperature (300 K). Increasing temperature yielded little change in the value of the conductance although the slope became smeared at higher temperatures. These observations imply that even at room temperature only a single 1-D subband is occupied and that transport through the Ge/Si nanowire remains ballistic; that is, the mean free path exceeds the channel length of 170 nm for this device. The results are consistent with the expected suppression of acoustic phonon scattering in 1-D systems due to the reduced

phase space for backscattering [72] and were confirmed by calculations using the Fermi's golden rule approach [5], although a more detailed theoretical analysis including the confinement effects of phonon modes may be needed to quantify the experimental data.

Multiple 1-D subbands in the Ge/Si nanowire system becomes accessible when the Fermi level inside the channel crosses higher subbands at increased gate or S/D voltage [Fig. 4(c)] [5], [73], [74]. In addition, many of the important features first observed in clean GaAs/AlGaAs systems, including the formation of half plateaus at high biases and the 0.7 structure at zero bias, were found in the Ge/Si system at relatively high temperatures. To this regard, the heavier effective mass of holes in the Ge/Si nanowire system will lead to a larger interaction parameter [75], [76], this together with a strong and uniform confinement potential along the channel and the ability to reliably produce transparent contacts should make the Ge/Si nanowire system an ideal platform to study the rich physics in strongly interacting systems.

2) Quantum Devices: In one of these studies of devices based on quantum coherence, the undoped Ge/Si core/shell NW heterostructure was contacted by a pair of superconducting (SC) leads [77]. Like conventional Josephson junctions in which a normal metal is sandwiched by two SC leads, proximity-induced superconductivity was observed in the SC/NW/SC device leading to a dissipationless supercurrent [Fig. 4(d)] [78]. Unlike conventional Josephson junctions, however, the semiconducting NW channel allows the amplitude of the supercurrent to be adjusted by a gate voltage through tuning of the normal-state resistance [79]. In addition, the devices are of such high quality that the ideal limits of electron conduction predicted by theory are now within reach. For example, the critical supercurrent I_C was found to correlate well with the normal state conductance G_n of the nanowire device, and I_C/G_n was found to be only a factor of 3.6 away from the theoretical limit [79]. Furthermore, due to quantum confinement and the formation of quantized conductance in the Ge nanowire channel, I_C does not change continuously with the gate voltage but in steps, with the step size ΔI_C also only a factor of three away from the theoretical limit.

Besides the supercurrent branch, the high-quality devices allow the observation of additional peaks due to coherent backscattering of electron/hole pairs (Andreev reflection) at the semiconductor/superconductor interface [80]. Multiple Andreev reflection peaks up to order 25 were observed [77], suggesting carriers can move freely through the devices up to 25 times without being backscattered inside the channel and once again demonstrating the near-perfect nature of the Ge/Si nanowire. The ability to create and control coherent SC ordered states in semiconductor-superconductor hybrid nanostructures further allows for new opportunities in the study of fundamental low-dimensional superconductivity. For example, the supercurrent devices can be thought of as a type of transistor device with strong nonlinear effects. In addition, new theoretical and experimental studies are required to explain the non-"classical" effects observed in the experiment such as the missing peaks and the anomalously high-amplitude of the higher order Andreev reflection peaks [77].

In another remarkable demonstration of quantum devices based on the Ge/Si core/shell nanowire system, coupled quantum dots were electrostatically formed inside a Ge/Si nanowire through a series of lithography-defined gates [81]. By tuning the barrier height between the dots through a gate voltage, coherent overlap of the charge (and spin) states in neighboring dots was achieved in a controllable fashion. Significantly, the charge states in the dots and the coupling between them were detected *in situ* using an integrated charge sensor in the form of a third quantum dot configured in another Ge/Si nanowire located more than 1 μm away. Clear charge signals were detected by the nanowire-based quantum dot detector even after direct transport measurements could no longer be carried out in the coupled dots [81]. The clean signals in this experiment clearly illustrate the near-ideal performance of the quantum dots defined in the nanowires and the excellent sensitivity of the charge sensing setup. The demonstration of coupled quantum dots and integrated sensing devices in turn paves the way for future studies on quantum computing schemes using 1-D systems like nanowires. In particular, compared to commonly used III–V systems, the Ge/Si nanowire system offers potential for longer spin coherence times due to the suppression of hyperfine interactions and, thus, a clear advantage for quantum devices based on a linear 1-D architecture.

3) Transistors—Performance and Scaling: The ability to obtain clean conduction channels and transparent contacts allows the fabrication of high-performance devices based on the Ge/Si nanowires. In conjunction with high-κ gate dielectrics (HfO_2 or ZrO_2) and metal top gate electrodes, we have shown that these nanowire devices can indeed outperform state-of-the-art CMOS devices and can operate within 90% of the ballistic limit at room temperature [6], [70]. Representative I_d–$V_{\rm gs}$ data obtained from a partially wrapped top-gate structure device with a channel length $L = 1$ μm [Fig. 5(a)] shows that the NW-FET has a peak transconductance, $g_m = dI_d/dV_{\rm gs}$, of 26 μS, and a maximum drain current $I_{d\,\max}$ of 35 μA at $V_g = -2$ V. Even better performance was achieved for a 190-nm channel length with $g_m = 60$ μS and $I_{d\,\max} = 91$ μA. In order to make a fair comparison with planar devices, the NWFET performance metrics were defined following the benchmarking method proposed by Intel [82], [83]. Specifically, $I_{\rm on}$ and $I_{\rm off}$ are defined as values at $V_{\rm gs}({\rm on}) = V_T - 0.7\,V_{\rm dd}$ and $V_{\rm gs}({\rm off}) = V_T + 0.3\,V_{\rm dd}$, so that 30% of the $V_{\rm gs}$ swing above the threshold voltage V_T is allocated to turn the device off, while the remaining 70% sets the operation range of the on state. Using this convention, $g_m = 60$ μS, $I_{\rm on} = 37$ μA($V_{\rm dd} = 1$ V) were obtained for the 190-nm channel length device. Using the total nanowire diameter (18 nm) as the device width, these values correspond to scaled g_m and $I_{\rm on}$ values of 3.3 mS/μm and 2.1 mA/μm, which are 3–4 times better than the values of 0.8 mS/μm and 0.71 mA/μm reported in state-of-the-art, sub-100 nm silicon p-MOSFETs employing high-κ dielectrics [84].

Recently, we have further demonstrated scaling of Ge/Si nanowire devices in studies of devices with channel length down to $L = 40$ nm [70]. To suppress screening of the gate fields by the microscale metal S/D leads in these sub-100-nm devices, integrated nanoscale contacts were fabricated by converting selected portions of the Ge/Si nanowire into metallic

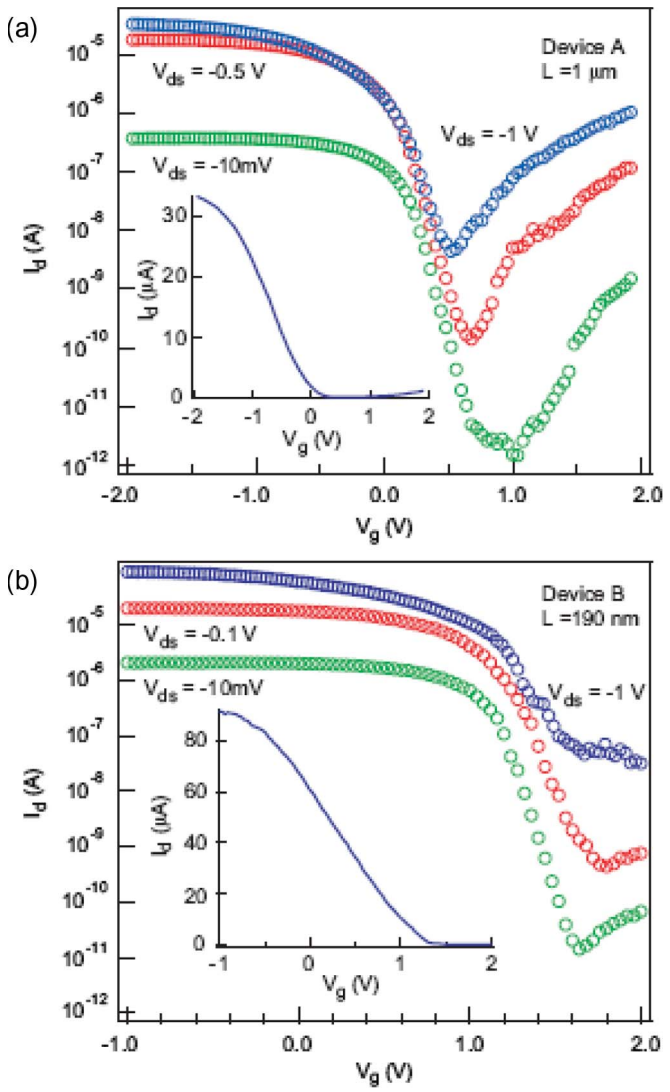

Fig. 5. I_d–V_g data for (a) $L = 1$ mm and (b) $L = 190$ nm Ge/Si NWFETs, where blue, red, and green data points correspond to $V_{\rm ds}$ values of -1, -0.5, and -0.01 V, respectively. Insets, linear scale plot of I_d versus V_g measured at $V_{\rm ds} = -1$ V. Adapted from [6].

$NiGe_xSi_y$ alloy through solid-state reaction of Ni with Ge/Si [Fig. 6(a)] [65], [70]. The excellent electrostatic integrity in these sub-100-nm nanowire devices with nanoscale S/D leads and ultrathin nanowire channel was confirmed with experimental results [Fig. 6(b)] and verified with EM simulations. For example, the subthreshold slope $S = [d(\log_{10} I_d)/dV_g]^{-1}$ was measured to be 160 mV/dec for the $L = 40$ nm NWFET at $V_{\rm ds} = -1$ V. Furthermore, increasing $V_{\rm ds}$ has little effect on the threshold voltage and subthreshold slope indicating effective suppression of the SCE. Notably, the scaled transconductance and on-current values for a gate and drain bias voltage window of 0.5 V were 6.2 mS/μm and 2.1 mA/μm for the 40-nm device and exceed the best reported values for planar Si and NW p-type FETs.

The performance of the Ge/Si nanowire devices have also been compared to planar Si devices using the intrinsic gate delay benchmark [82], $\tau = CV/I$, where C is the gate capacitance, $V = V_{\rm dd}$, and I is the on current $I_{\rm on}$. As defined, τ is relatively insensitive to the gate dielectric and device width and, thus, represents an important parameter for comparing different types of devices [85]. The Ge/Si nanowire FETs were found to show clear speed advantage at a given L versus Si p-MOSFETs over the entire range of devices studied [Fig. 6(c)]. For example, the 2-THz intrinsic speed ($\tau = 0.5$ ps) indicated for the 40-nm device represents the highest frequency among nanowire FETs and p-MOSFETs [82] and is comparable to the best value observed for carbon nanotube FETs [82], [86]. This observation is consistent with transport studies which revealed a hole mobility $\mu = 730$ cm^2/V $\cdot$ s [6], more than a factor of ten higher over that of Si pMOSFETs with HfO_2 gate dielectric ($50 \sim 60$ cm^2/V $\cdot$ s) [84] and also more than twice that reported for Ge and strained SiGe heterostructure PMOS devices [87], [88]. Moreover, the plots show that length scaling of τ is more favorable for the Ge/Si NW-FETs than Si MOSFETs [6] with a slope of $\sim$1.5 versus $\sim$1.1, respectively. Since a slope of two is expected for ideal constant-voltage scaling, the nonideal performance can mostly be attributed to reduced mobility due to surface scattering in planar devices at high fields [85]. The relatively constant mobility observed for Ge/Si NWFETs [6] suggests that the epitaxial cylindrical Si shell results in excellent passivation that along with the smooth nanowire surface suppresses surface scattering in these ultrathin body devices.

The suggestion that scattering is suppressed in quasi-1-D Ge/Si nanowires has been evaluated by determining how close these FETs are to the scattering-free ballistic limit [70], [89], [90]. Analysis of the transport behavior of Ge/Si nanowire FETs using a semiclassical ballistic transport model coupled with a $sp^3d^5s^*$ tight-binding model to describe the electronic structure of Ge NW core [70], [89], [90] demonstrates that the calculated and experimental I_d–$V_{\rm gs}$ transfer characteristics [Fig. 6(b)] show very close agreement. For drain voltages up to -0.1 V, the sub-100-nm channel length devices deliver dc current close to the ballistic limit, while even at a higher bias of $V_{\rm ds} = -0.5$ V, the simulation results suggest that the $L = 40$ nm devices operate at 90% of the ballistic limit at room temperature.

C. n-Channel Heterostructure Nanowires

Analogous to the 1-D hole gas formed in the Ge/Si core/shell nanowires, 1-D electron gases and high-performance n-channel NWFETs were demonstrated in nanowire radial heterostructures by exploring the conduction band offset in selected materials. For example, undoped GaN/AlN/AlGaN radial nanowire heterostructures show the formation of an electron gas inside the GaN core [16] due to strong spontaneous and piezoelectric polarization [91]. Precise control of both the shell thickness and composition during MOCVD nanowire growth process [16], [17], [92] allows fine tuning of the bandstructure and, more importantly, the formation of near-ideal atomically sharp interface between the core and shell layers [Fig. 7(a)]. In addition, a precisely controlled 2-nm AlN interlayer was grown between the GaN core and AlGaN outer shell to provide a larger conduction band discontinuity for better confinement of electrons and to reduce alloy scattering from the AlGaN outer shell [93].

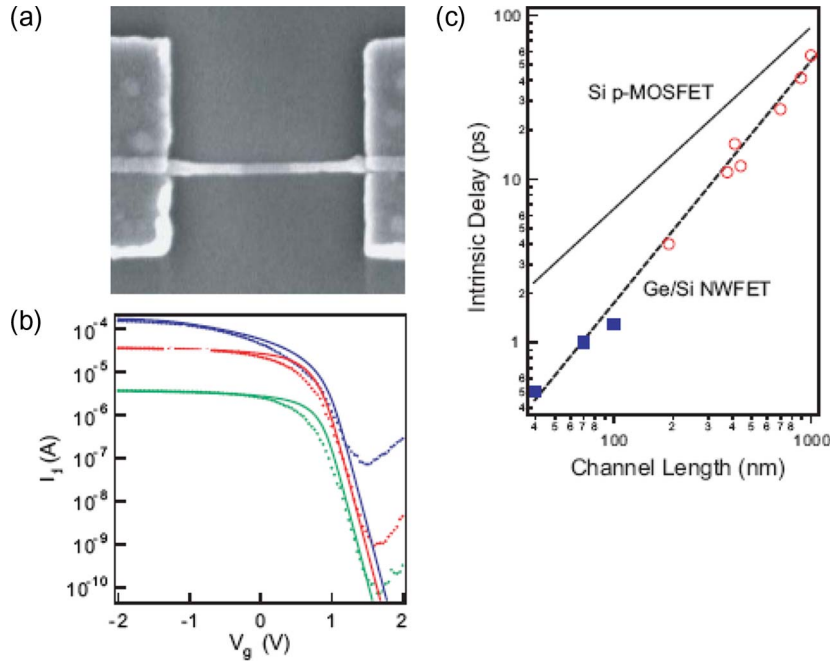

Fig. 6. (a) SEM image of a $L \sim 100$ nm Ge/Si NWFET with Ni(Ge/Si) nanowire S/D connections. (b) Comparison of simulated and measured transfer characteristics for a $L = 40$ nm Ge/Si NWFETs. Symbols are experimental data and solid lines are ballistic simulations. Green, red, and blue data points correspond to $V_{\rm ds} = -10$, -100 and -500 mV, respectively. (c) Length dependence of intrinsic delay for Ge/Si NWFETs compared with Si p-MOSFET results. Adapted from [70].

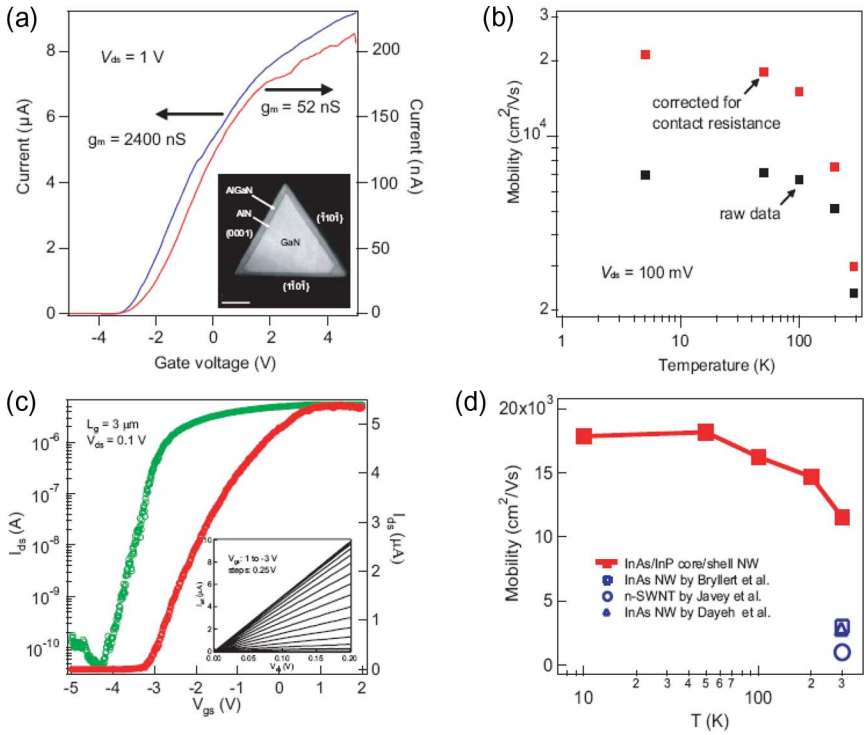

Fig. 7. (a) Transfer characteristics for (blue) a GaN/AlN/$Al_{0.25}Ga_{0.75}N$ nanowire heterostructure and (red) a GaN nanowire. Inset is HAADF-STEM cross-sectional image of a GaN/AlN/AlGaN nanowire; scale bar, 50 nm. (b) (Black) Measured and (red) intrinsic temperature-dependent electron mobility for a GaN/AlN/$Al_{0.25}Ga_{0.75}N$ nanowire. (c) I_d–$V_{\rm gs}$ data for a InAs/InP top-gated NWFET with $L = 3$ μm. Inset shows I_d–$V_{\rm ds}$ data recorded at $V_{\rm gs}$ values from $+1.0$ to -3.0 V. (d) Temperature-dependent electron mobility of an InAs/InP nanowire and highest room-temperature electron mobility values reported in other 1-D nanostructures. Adapted from [15] and [16].

Transport measurements carried out on the GaN/AlN/AlGaN heterostructure nanowires and GaN nanowire control samples demonstrate the formation of an electron gas in the undoped GaN/AlN/AlGaN nanowire heterostructures with significant improvement in terms of carrier mobility and device performance. For example, intrinsic electron mobilities of 3100 and 21 000 $\rm cm^2/V \cdot s$ were obtained at room temperature and 5 K, respectively, for the heterostructure nanowire [Fig. 7(b)]

[16]. Moreover, devices fabricated with ZrO_2 dielectrics and metal top gates showed excellent n-FET performance with scaled on-current and transconductance values of 500 mA/mm and 420 mS/mm, respectively [16]. A near ideal subthreshold slope of 68 mV/dec and an on/off current ratio of 10^7 were obtained for the 1-μm-long device, demonstrating the excellent interfacial properties and electrostatic control.

More recently, the rational design and synthesis of InAs/InP core/shell NW heterostructures with quantum-confined high-mobility electron channels have been reported [15]. InP is an attractive shell material because the conduction band offset of $\sim$0.52 eV provides a good confinement potential for electrons, and because the type-I quantum well structure also confines holes that may be thermally generated or resulted from impact ionization in the channel [94]. Transmission electron microscopy studies revealed single crystal InAs cores with epitaxial InP shells 2–3 nm in thickness, and energy-dispersive X-ray spectroscopy analysis further confirmed the composition of the designed heterostructure. Room-temperature electrical measurements on InAs/InP nanowire FETs showed significant improvement in the on-current and transconductance compared to InAs nanowire FETs fabricated in parallel. For example, the transconductance values show an approximately fivefold increase for InAs/InP (2.2 μS) versus InAs (0.45 μS), which corresponds to a substantially enhanced electron mobility.

The temperature-dependence of the field-effect electron mobility [Fig. 7(d)] shows that the electron mobility of the InAs/InP nanowire devices increases from 11 500 $\mathrm{cm}^2/\mathrm{Vs}$ at room temperature, and then saturates at 18 000 $\mathrm{cm}^2/\mathrm{Vs}$ for $T < 100$ K. It is worth mentioning that contact resistance was not taken into account in this analysis, and thus higher mobility values could be achieved by subtracting this series resistance term and/or optimization of contact transparency. Our data can also be compared to recent electron mobility values reported in other n-channel nanowire and carbon nanotube devices [Fig. 7(d)] calculated using a consistent charge-control model. The 11 500 $\mathrm{cm}^2/\mathrm{Vs}$ room-temperature electron mobility in our InAs/InP nanowire heterostructures, which represents a lower bound value without contact resistance correction, is significantly higher than reported electron mobility data for these other 1-D nanostructures and, thus, further substantiates the promise of the radial core/shell approach for creating unique nanoscale building blocks.

InAs/InP nanowire devices with a top metal gate structure incorporating high-κ dielectric were fabricated to explore the potential as high-performance FETs. The I_d–V_{gs} transfer curve recorded at $V_{\mathrm{ds}} = 0.1$ V exhibits a peak transconductance of ~ 3.0 μS and a subthreshold slope of $\sim$180 mV/dec for a $L = 3$ μm device. Representative transfer curves recorded from $L = 170$ nm device show an on–off ratio ($> 10^5$) and $S \sim 80$ mV/dec for $V_{\mathrm{ds}} = 10$ mV, although these values decreased/increased to 10^3/260 mV/dec as V_{ds} increased to 0.5 V. This trend indicates a nonnegligible SCE. Notably, the scaled values of the on-current, 3.2 $\mathrm{mA}/\mu\mathrm{m}$, and transconductance, 2.5 $\mathrm{mS}/\mu\mathrm{m}$, are substantially higher than other n-channel nanowire and nanotube FETs [16], [86] and exceed n-channel Si MOSFETs [95].

IV. Integration Techniques

To fulfill the potential of nanowires as building blocks for future electronics, effective integration and assembly techniques must be developed to transfer the nanowires from growth substrates onto their respective device substrates, and to arrange large numbers of nanowires into complex integrated circuits. The requirements are twofold: First, methods are needed to assemble nanowires into highly integrated arrays with controlled orientation and spatial position; second, approaches must be devised to access NW device on multiple length scales and to make interconnects between the nano-, micro- and macroscopic subsystems.

Several methods have been developed to address the first requirement to produce parallel nanowire arrays. In essence, these approaches employ an external force to preferably align the nanowires in a preselected direction during the assembly process; for example, electrostatic force in the case of electric field directed assembly [21] and shear force in the case of fluid-assisted assembly [96], [97] processes. In fluid-assisted assembly, the average NW surface coverage can be controlled by the flow duration while the alignment can be improved by increasing the flow rate due to higher shear force. The size of the aligned nanowire array is limited only by the size of the fluidic channel being used and can readily be extended to over hundreds of micrometers. Furthermore, more complex crossed NW structures can be obtained with the fluidic flow assembly approach by alternated flow in orthogonal directions in a layer-by-layer assembly process [97].

Two additional fluid-based methods have been demonstrated to organize nanowire building blocks *en masse*: the Langmuir–Blodgett (LB) technique at the centimeter level [31], [98], [99] and the blown-bubble method at the wafer level [100], [101]. In the LB process [102], a nanowire-surfactant monolayer is uniaxially compressed on an aqueous subphase thereby producing aligned nanowires with controlled spacing. The compressed layer is then transferred in a single step to a planar substrate to yield parallel NWs covering the entire substrate surface [31]. The spacing of the transferred NWs can be controlled from micrometer scale down to close-packed structures during the compression process [31]. Fine tuning of the nanowire spacing can be further achieved through the use of sacrificial shell layers that are subsequently removed after assembly into close-packed structures [31], [103], thereby yielding nanowire arrays with variable density.

Analogous to the fluid flow assembly but using the shear stress generated during the expansion of a film, aligned nanowire films were demonstrated at the wafer scale or larger using the blown bubble film (BBF) approach [100], [101]. The BBF approach involves the preparation of a homogeneous solution containing dispersed nanowires or nanotubes, expansion of a bubble from the nanomaterial solution at a controlled direction and speed, and subsequent transfer of the bubble to receiving device substrates. Nanowire films with density up to 10^6 cm^{-2} have been demonstrated on 8-in wafers with the angular spread less than 10° over the entire wafer. The nanowire density was limited by aggregation in high-density solutions and may be further improved through optimization of surface

chemistry. Considering that every year several billion pounds of polymers are processed into plastic products (e.g., bags, films) by the blown film extrusion technique, the BBF approach may provide a realistic route to produce large-scale NW-based electronics at a reasonable cost.

In all of these approaches, repetition of the nanowire alignment/transfer process one or more times can produce crossed and more complex nanowire structures on virtually any substrate from crystalline Si to flexible plastics. To this end, another promising approach recently has been reported that involves a dry deposition strategy on substrates up to wafer scale [104], [105]. The overall process involves optimized growth of designed nanowire material followed by transfer of nanowires directly from the growth substrate to a second device substrate via contact printing. Key features of this process include the ability to print aligned NWs on a wafer scale and to control the density of aligned NW through the transfer process. In addition, similar to the solution-based assembly techniques, the transfer method is readily adaptable to 3-D structures.

Distinct from the precise device control that can be achieved in conventional top–down fabrication, bottom–up assembly methods typically result in excellent pitch and orientation control but little control of the end-to-end registry between nanowires. This process variation, however, may not fundamentally limit the application of nanowire-based electronics. For example, by adjusting the channel length to be less than the average NW length, it is possible to minimize the number of NWs that fail to bridge the S/D contacts. In addition, just as the concept of integrated circuits greatly speeded up the development of CMOS technology, the emergence of new architectures, such as the crossbar structure that will be discussed in Section V, may maximize the opportunities offered by the 1-D nanowire systems and lead to high-density high-performance applications. Furthermore, the ability to create aligned nanowire arrays on diverse substrates in turn makes the bottom–up approach well-suited for applications based on thin-film transistors (TFTs) such as flexible and/or transparent electronics on plastic or glass substrates. The high-quality crystalline nanowire channels in the nanowire-based TFTs offer much improved device performance compared with conventional approaches, a topic that will be discussed in Section V. Compared with single-nanowire-based devices, the nanowire-TFT devices consist of aligned arrays of nanowires thus effects caused by assembly/integration process variations can be further mitigated due to averaging effects.

Contrary to the solution-based or dry-transfer techniques, nanowire integration can also be realized through direct growth at selected sites, typically from an exposed (111) silicon surface [106], [107] in the case of Si nanowires and on InAs (111)B surfaces in the case of InAs nanowires [38]. The main advantage of this "grow-in-place" method is the additional control of the end-to-end registry. On the other hand, in these approaches the growth substrate normally also serves as the device substrate which poses limit on the possible choice of substrate material, although device fabrication on diverse substrates may be achieved through additional transfer processes while maintaining the position registry [108]. Two types of growth modes have been explored. In the vertical growth approach, nanowires are grown epitaxially from a suitable substrate and form vertically aligned arrays. Using the growth substrate as the source electrode and deposited thin-film drain and gate electrodes, vertical nanowire-transistors (VNWFETs) have been demonstrated [41], [109], [110] and may offer increased on-current due to the use of gate-all-around structure. By placing the surround gate asymmetrically between a p-type drain and an n-Si source, impact-ionization MOS operation was also demonstrated on VNWFETs in which subthreshold slope as low as 5 mV/dec was obtained in the OFF-state [111]. In the horizontal growth approach, nanowires are grown across prefabricated trenches, which are also used as the source/drain electrodes [107]. This approach has led to the demonstration of single-crystalline nanowire bridges [107] and nanoelectromechanical devices [112], [113].

There are also challenges for VNWFET devices where all the transistors share a single source electrode (the growth substrate), including the design and fabrication of high-density integrated circuits, and the demonstration of effective integration methods with existing planar structures. Likewise, challenges remain for horizontal epitaxial growth, since little control has been demonstrated in terms of the nanowire position and density.

V. Nanowire Circuits

A. NW Crossbar Circuits

One obvious approach to incorporate high-performance nanowire devices is by replacing planar silicon elements in conventional integrated CMOS circuits. Because this approach requires the assembly of billions of nanowires with precise positional registry at the single nanowire level, it remains both a daunting task and one that does not necessarily take advantage of the unique opportunities offered by the 1-D nanomaterials. Specifically, the elongated nanowire structure with aspect ratios well above 10^3 should offer new possibilities for effective circuit integration at the nanoarchitecture level, where large numbers of devices are linked with each other and with external systems to perform certain memory and/or logic functions, as well as at the system architecture level. One interesting candidate architecture that can exploit the unique properties of the 1-D nanowire structure is the crossbar structure (Fig. 8) [114]–[120], where active devices are formed at the intersection points of two sets of crossed nanowires. This motif offers high device density and efficient interconnects between individual devices and functional device arrays. In addition, a reconfigurable crossbar structure allows for effective incorporation of defect-tolerant computing schemes, a necessity for bottom–up-based devices since traditional near defect-free oriented processes will not likely be feasible at the deep nanometer length scale [121].

In an earlier proof-of-concept study, we demonstrated prototype logic circuits using crossed nanowire p-n junctions and fluid-assisted alignment technique [21], [23]. For example, a two-input two-output AND logic gate was assembled from 1(p-Si) $\times$ 3(n-GaN) multiple junction arrays in which the crossed Si and GaN nanowires operate as p-n junctions.

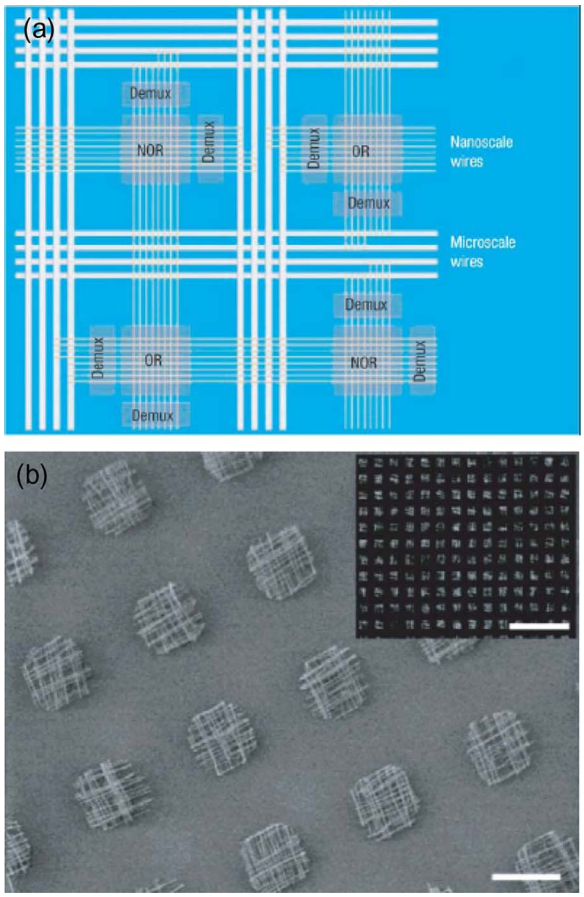

Fig. 8. (a) Crossbar nanowire architecture for computing. (b) SEM image of patterned crossed nanowire arrays produced by LB method; scale bar is 10 μm. Inset shows larger area optical image of the nanowire crossbar array; scale bar is 100 μm. Adapted from [31] and [120].

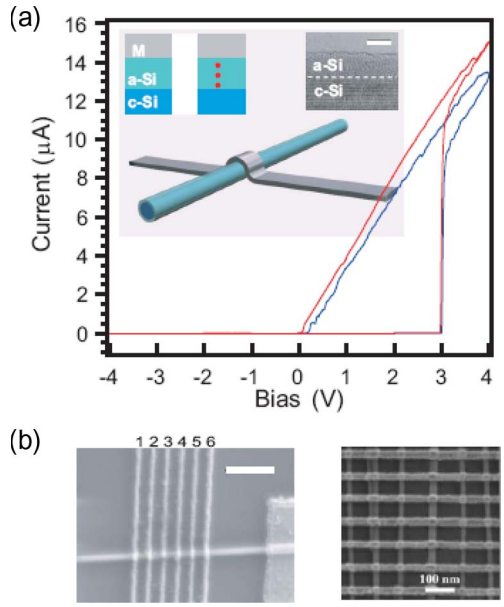

Fig. 9. (a) Hysteretic diodelike resistance-switching observed at a crosspoint. The initial cycle is shown in red and subsequent cycles are in blue. Main inset: schematic of the crossbar memory formed by (rows) metal wires and (columns) core-shell nanowires made of c-Si/a-Si. (Top left) Schematic of a single memory bit showing metal and c-Si electrodes sandwiching an a-Si shell. (Top center) Formation of a metal filament inside the a-Si layer changes the memory bit from the high to low resistance state. (Top right) TEM image of a c-Si/a-Si core-shell nanowire. Dashed line indicates the interface between the c-Si and a-Si. Scale bar, 5 nm. b, Left panel: SEM image of a 1 $\times$ 6 crossbar array fabricated on a single nanowire with 30-nm metal linewidth and 150-nm spacing. Right panel: SEM image of a 2-D crossbar memory with 100-nm pitch. Adapted from [122].

Logic-0 is observed from this device when either one or both of the inputs are low due to pull-down of the forward-biased p-n junction and logic-1 is observed only when both inputs are high. Multi-input FET-based NOR logic gates were also demonstrated using a different configuration of assembled 1(p-Si) $\times$ 3(n-GaN) crossed NW-FET arrays in which the GaN nanowires serve as gates of the Si NWFET [23]. The logic-0 is observed when either one or both of the inputs are high and logic-1 state can only be achieved when both gated regions of the Si NWFET are on; that is, both inputs are low. In addition, analysis of the $V_o - V_i$ data demonstrates that these two-input NOR gates routinely exhibit gains in excess of five, which is a critical characteristic since it enables interconnection of arrays of logic gates without signal restoration at each stage.

The nanowire crossbar motif offers a universal paradigm for both logic and memory functions. For example, based on the demonstrated NOR operation in crossed nanowire field-effect devices [21], [23], DeHon [115] proposed that programmable-logic arrays (PLAs) can be built using nanowire FET NOR planes [Fig. 8(a)]. General logic computing can be achieved in an array-based architecture such that the output from one array forms the input of the other through crossbar interconnects [115], [118]. Programming of the FET-based arrays will likely be implemented during the fabrication stage through controlling the threshold voltage V_T at selected transistor regions, for example, by introducing modulation doping along the nanowire or by modulation of the gate oxide thickness [10].

The hierarchical patterning of arrays of aligned and crossed nanowires needed to realize such PLA architectures can be implemented using the fluid-assisted or dry-transfer assembly methods discussed earlier. For example, parallel arrays of nanowires in which the average nanowire separation, array dimensions, and array pitch have been controlled over entire substrates by combination of the LB approach and conventional photolithography [31]. Nanowire crossbar arrays have been further obtained by the sequential transfer and patterning of a second layer of nanowires in the orthogonal orientation [31], [103]. An image of regularly patterned 10 $\times$ 10 μm square arrays with a 25 μm array pitch is shown in Fig. 8(b) and demonstrates that such a method provides ready and scalable access to ordered arrays over large areas. The nanowire arrays exhibits order on multiple length scales: 40-nm diameter NWs, 0.5-μm NW spacing, 10-μm array size, 25-μm array pitch repeated over centimeters.

In addition to field-effect devices, nanowire core/shell structures designed to function as reconfigurable diode switches that can be used in memory and wired-OR operations have been reported [117], [119]. For example, by growing nanowires with p-type crystalline-silicon (c-Si) cores and amorphous-silicon (a-Si) shells, we have recently observed hysteretic resistance switching at c-Si/a-Si core/shell nanowire—metal nanowire crosspoints in which the a-Si layer acts as the information storage medium (Fig. 9) [122]. The resistance switching was

attributed to metal filament formation (retraction) inside the a-Si matrix to yield high (low) conductance ON (OFF) states [123] [inset, Fig. 9(a)]. The a-Si/c-Si core/shell nanowire system offers reliable resistance switching and ~100% yield down to at least 20 × 20 nm (limited by the size of the nanowire and lithography resolution), corresponding to a potential device density better than 6×10^{10} bits/cm^2. As a nonvolatile memory device, this core/shell nanowire system shows large ON/OFF ratio ($> 10^4$), low programming current (~ 10 μA), fast programming speed ($<$ 100 ns) and long endurance cycles (10^5). The retention time (~2 weeks) will likely be improved as the devices are optimized as retention $>$ 2 years was observed in microscale planar nanoscale planar p-Si/a-Si/metal structures [124]. Another interesting feature of the devices is that they exhibit intrinsic rectification: the device at ON state shows asymmetric I–V resembling that of a diode [Fig. 9(a)] rather than a resistor. The rectifying I–V at ON state is desirable for crossbar-based circuits as it mitigates crosstalk between elements [125], [126]. Indeed, the bits in multielement 1-D and 2-D crossbar arrays [Fig. 9(b)] can be written, read and rewritten in a fully independent manner [122].

B. Bridging the Nano- and Micro-Worlds

In the crossbar circuit [Fig. 8(a)], address demultiplexers serve as a needed interface that bridges the very large number of nanowires used in each crossbar array with a limited number of conventional, microscale control wires. By definition, address demultiplexers are logic circuits that specifically select and transmit signals to a single output wire based on each address code. In principle, it only requires n pairs of address wires to select and control 2^n nanowires, e.g., ten pairs of address wires can possibly control 1024 (2^{10}) nanowires. As a result, 20 pairs of address wires might be sufficient to completely address a 1-Mb crossbar memory [115] through a pair of well-designed address demultiplexers.

An address demultiplexer can be realized using the wired-NOR operation in a "mixed" crossbar array formed by microscale control wires and the nanoscale signal nanowires. Address selection can be achieved by coding the nanowires in the mixed array (e.g., disabling certain cross-points through modulation doping along the nanowire axis) such that the desired nanowire can be activated (selected) only by the right combination of the address inputs. Furthermore, it can be shown that if the coded nanowires are chosen at random from a sufficiently large population, a large fraction ($>$ 99%) of the selected nanowires will have unique addresses even without knowledge of the specific locations of the coded regions [116]. Such a stochastic decoding scheme is ideally suited for nanowire crossbars formed via the bottom–up assembly techniques, since during the assembly (fluid-assisted or dry-transfer), the registry of the nanowires is generally lost, resulting in arrays of aligned albeit randomly positioned nanowires.

The first prototype nanowire demultiplexer was demonstrated using crossed nanowires in which coding of the nanowires were achieved through surface modification at selected cross-points [127]. However, this method relied on electron beam lithography to selectively functionalize desired

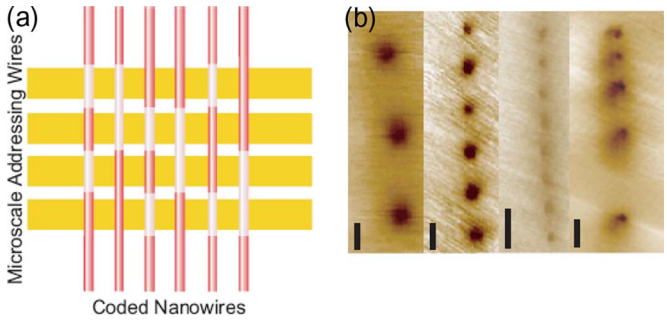

Fig. 10. (a) Schematic of demultiplexer based on synthetically coded nanowires (b) SGM images of $n^+ - (n - n^+)_N$ nanowires where left-to-right are $N = 3$, $N = 6$, $N = 8$, and $N = 5$ nanowire devices. The growth times for the n/n$^+$ regions of the $N = 3$, 6 and 8 were 1/3, 1/1, and 0.5/0.5 min, respectively. The growth times for the n regions of the $N = 5$ device are 0.5 min, and for the n$^+$ sections are 0.5, 1, 2, and 4 min. Scale bars are 1 μm. Adapted from [10] and [120].

cross-points. More recently, coding along a nanowire was achieved via bottom–up synthesis alone without the assistance of top–down lithography [10]. Coding was accomplished via modulation doping of the nanowires such that only lightly doped regions would be affected by the microscale control wires serving as gates, while the heavily doped regions would be insensitive to the control signal. Scanning gate microscopy (SGM) studies clearly verified that modulation doping was achieved along the nanowire axis with full control of the size, spacing, and number of the modulated regions during the growth process (Fig. 10). Functional mixed nanowire/microscale wire demultiplexer arrays were in turn demonstrated in which the only postgrowth lithographic steps involved making external input and output contacts to the few microscale control wires. The ability to encode information in the nanowires in a controlled fashion during growth has many analogies to biology where the information is encoded in a replicated DNA molecule, and opens opportunities to the ultimate integrated circuits—ultrahigh density nanocircuits exclusively produced via bottom–up self-assembly without involvement of top–down fabrication techniques.

C. Transparent and Flexible Electronics

Another potential application of nanowire-based electronics is devices on noncrystalline substrates such as plastics and glass. Devices made on these low-cost and lightweight substrates serve as the basis for a large and rapidly growing class of electronics applications, including flat-panel displays, smart cards, and wearable electronics [128]–[131]. However, due to the low thermal tolerance of these substrates, conventional TFTs are typically composed of amorphous materials such as amorphous-silicon (a-Si) or organic semiconductors and have low mobility ($\sim 0.1 - 1$ cm^2/V $\cdot$ s) and speed ($<$ kHz). In the nanowire-TFT approach, high-quality crystalline nanowire materials are transferred from the growth substrate to a separate receiving device substrate, and high-performance devices are fabricated with standard low-temperature processes on the transferred crystalline materials (Fig. 11) resulting in much higher mobility and device performance. Furthermore, although comparable mobility may be obtained on polycrystalline silicon

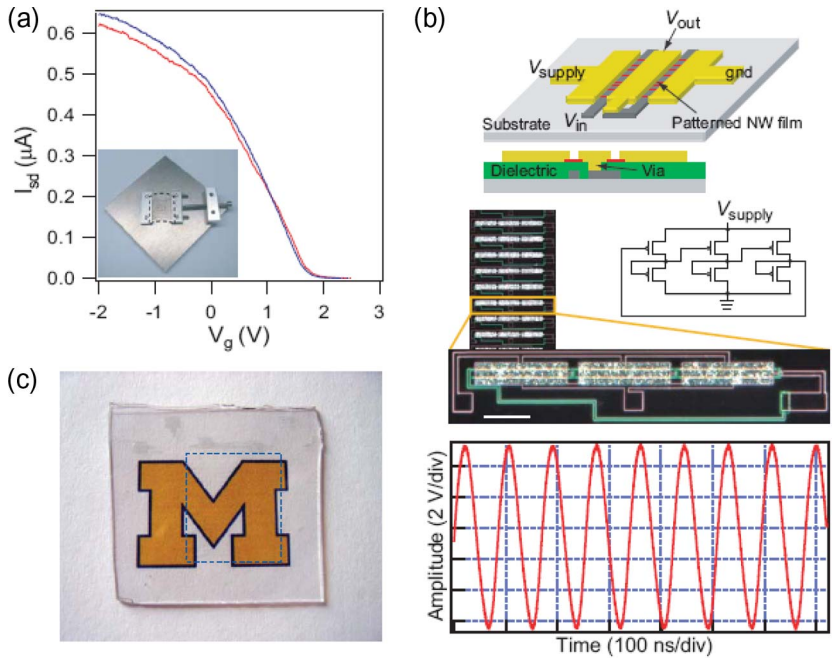

Fig. 11. (a) $I_{\rm sd}$ versus V_g for a NW transistor device measured when the substrate was (blue curve) flat and (red curve) bent to a radius of curvature of 0.3 cm. (Inset) A photograph of the device used for bending the flexible plastic chip and securing it during measurement. The chip is highlighted with a black dashed line. (b) (Top) Schematics of the multinanowire inverter unit used in the ring oscillator. The dielectric is omitted in the perspective schematic for clarity. (Middle) Optical images and circuit diagram of nanowire ring oscillators. Scale bar is 100 μm. (Bottom) 11.7-MHz oscillation in a ring oscillator. (c) Digital photograph of a 200-device array of nanowire TFTs fabricated on 500-μm-thick glass. The logo of the University of Michigan can clearly be seen through the nanowire array indicated by dashed square. Adapted from [58], [134], and [135].

devices, the additional steps and higher temperature processing required to achieve high-quality polycrystalline silicon represent limitations in the implementation of polycrystalline silicon transistors on large-scale glass and plastic substrates [131].

One key advantage of the nanowire TFT approach is the ability to decouple the high-temperature material growth stage from the low-temperature device fabrication stage. In the first stage, the synthesis of nanowire building blocks is carried out under conditions optimized to yield high-quality single-crystalline materials, where the desired electronic and/or photonic functions are defined by material composition, structure, and diameter. In the device fabrication stage, the nanowires are transferred to a specified plastic or glass substrate using solution- or dry-based transfer/alignment methods discussed earlier, followed by device patterning at low temperatures only. In this regard, nanowires offer the same processing advantages as organic semiconductors [132], [133], while providing significantly improved device performance.

Following this approach, logic, memory, and photonic devices on glass and plastic substrates have been demonstrated using single-crystalline Si, SnO_2, Ge/Si, and GaN nanowires [58], [134], [135]. For example, TFTs based on Si nanowires exhibited mobility values, 200–300 $\rm cm^2/V \cdot s$, independent of the substrate due to the clear separation of growth and device fabrication stages. Notably, these values are two–three orders better than that obtained in amorphous Si or organic devices [136]–[138]. The performance of devices fabricated on a plastic substrate shows little degradation when bent [134], verifying the potential of nanowire-based devices in applications such as flexible electronics [Fig. 11(a)]. In addition, treating aligned nanowires as a thin-film material allows integrated circuits to be fabricated using conventional techniques. For example, a three-stage ring oscillator composed of more than 100 nanowires was demonstrated with an oscillation frequency of circa 11 MHz on Si substrate [Fig. 11(b)] [135]. Contrary to conventional planar devices, which exhibit degradation in device performance when fabricated on noncrystalline substrates, the nanowire ring oscillators exhibited higher operating frequencies on a glass substrate. This observation can be attributed to the insensitivity of carrier mobility in nanowire devices to substrates, and reduction of the stray capacitance on the insulating glass compared to conducting Si substrates [135]. Using the same motif, the Rogers group at University of Illinois at Urbana–Champaign [139], [140] has demonstrated flexible circuits based on silicon nanoribbons etched from SOI source substrates and transferred onto stretchable polyimide device substrates. The array of devices demonstrated so far includes inverters, differential amplifiers and ring oscillators with stable oscillation frequency up to 3 MHz [140].

Recently, we have also reported fully transparent electronics on glass substrates [58] using wide bandgap materials such as SnO_2 nanowires as the TFT channel, along with sputtered transparent ITO source/drain and gate electrodes. The transparent TFTs show transmittance $> 80\%$, field-effect mobilities $> 100\ \rm cm^2/V \cdot s$ and on/off ratios $> 10^6$ within a low 4 V bias range. The high mobility in turn results in improved device speed. Direct radio frequency measurements on the transparent nanowire-TFTs using a two-port S-parameter setup show that unity current gain cutoff frequency f_T as high as 109 MHz, and power gain cutoff frequency $f_{\rm max}$ as high as 286 MHz can be obtained [141]. These operation speeds are already significantly higher compared with those obtained in other approaches to

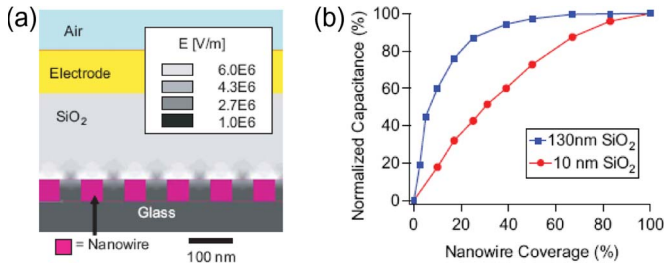

Fig. 12. (a) Distribution of the electrical fields in the cross section of a nanowire TFT with 50% nanowire coverage obtained through electrostatic simulation. (b) Gate capacitance of the nanowire TFT as a function of the nanowire coverage in the channel region at different dielectric thicknesses. The gate capacitance is normalized to the maximum value when the nanowire coverage is 100%. Adapted from [58].

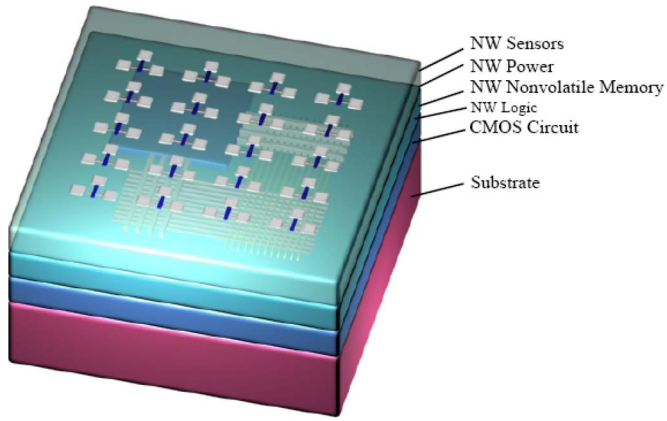

Fig. 13. Schematic 3-D multifunctional nanowire-based chip.

transparent electronics using organic semiconductors or conventional transparent metal-oxide films, where operation speed has been typically limited to the kilohertz range [142]–[144].

Device uniformity is a potential concern for systems based on the bottom–up paradigm. The controlled growth and doping of nanowires, which contrasts the current situation with carbon nanotubes, can yield similar electrical properties for nanowire samples [3], although variations in device uniformity can still arise due to fluctuations of the nanowire density at different locations within the circuit. Experimental and simulation studies on prototype nanowire TFTs show, however, that the device performance is in fact insensitive to the nanowire density above a certain threshold [58]. For example, for devices using 130-nm-thick SiO_2 as the gate dielectric, the gate capacitance C_g reaches 90% of that expected for a continuous film if the nanowire coverage is above 25% (Fig. 12). This observation can be attributed to the fact that above a certain threshold the nanowire array can effectively screen the field lines from the gate and effectively act as a continuous film [Fig. 12(a)]. Since the TFT device parameters such as drain current $(I_{\rm ds})$ and transconductance (g_m) are directly related to C_g, one can conclude that for nanowire coverage above a certain threshold fluctuations of the nanowire densities will have little effect on the TFT performance: If 10% on-current variation is required, 22% nanowire density variation between devices is allowed for a $T_{\rm ox} = 100$ nm when the nanowire coverage is $\sim$25%. The flexibility in density is tightened for thinner $T_{\rm ox}$ but even for $T_{\rm ox} = 30$ nm 23% nanowire density variation is permitted if the nanowire coverage is $\sim$50% [141]. These results show that nanowire uniformity is sufficient for TFT-based electronics, and suggest substantial opportunities for fabrication of more complex and larger scale circuits.

D. 3-D Heterogeneous Integration

As discussed earlier, the solution-based or dry transfer and assembly methods are readily adaptable to 3-D structures. Specifically, repeating the transfer process has enabled up to ten layers of active NW field-effect devices to be assembled, where uniform device performance was demonstrated from layers 1 through 10 [104]. In addition, a flexible bilayer structure consisting of logic in layer-1 and nonvolatile memory in layer -2 was demonstrated on a plastic substrate [104]. This capability and the ability to assemble virtually any nanowire material at will offers one of the strongest arguments for bottom–up approach in the future. For example, a multifunctional stand-alone system that consists of highly sensitive nanowire-based chemical or biological sensors at the top layer [145], integrated high-performance logic and memory components to process and store the data, and a nanowire-solar cell layer [146], [147] at the bottom that directly powers the sensor and logic circuits can be shown in Fig. 13. This type of 3-D heterogeneous system could be fabricated on top of a conventional CMOS-based circuit for added function, or on, for example, a flexible plastic substrate as a versatile, self-powered nanoelectronic system.

VI. Summary

Substantial progress has been made in defining the performance limits and exploring applications based on NWFETs and other nanowire-enabled devices prepared using the bottom–up paradigm [2], [3], [21]–[23]. Several key factors have contributed to this progress and heightened research interest in nanowire devices. First, semiconductor nanowires can now be prepared in high-yield with reproducible electronic properties for a variety of material compositions as required for large-scale integrated systems and different possible applications. Second, studies have now shown that bottom–up nanowire field-effect devices, which allow for better control of channel dimensions at the deep nanometer regime, can out perform the best devices made by top–down processing. Third, advances in large-scale assembly methods have allowed for the fabrication and testing of basic nanoelectronic circuits, the development of new nanowire-TFT-based devices, and exploration of 3-D multifunctional nanoelectronics.

Despite this encouraging progress, a continued focus of at least part of our research effort on addressing fundamental scientific questions will undoubtedly yield both expected and unexpected advances as we move nanowire devices and arrays from science to true technology. For example, advances in the controlled assembly could benefit virtually any area proposed for nanowire electronics. Yet, exploration of non-CMOS applications, such as flexible electronics, represents an area where technology is much closer and that could benefit from work pushing level of circuit sophistication and integration versus

basic device properties. It is also possible that a next-generation non-CMOS electronics, such as nonvolatile memory, could still have substantial CMOS components in it: Built by hybrid bottom–up/top–down structures at the physical device level, and operated with crossbar/CMOS structures at the architecture level.

As one looks further out to the future, we expect many opportunities to arise where the bottom–up approach could open up unique science and technology from top–down approaches for nanoelectronics. Such area includes the development of 3-D multifunctional nanoelectronics, where the capability of assembling distinct nanowire building blocks in multiple active layers is uniquely enabled by the bottom–up approach, as well as hybrid nanoelectronic/biological systems, where the capability of fabricating devices on flexible, biologically compatible substrates could open up unique opportunities for the future.

REFERENCES

[1] ITRS Organization, *International Technology Roadmap for Semiconductors Report 2007 edition*, 2007.

[2] C. M. Lieber and Z. L. Wang, "Functional nanowires," *MRS Bull.*, vol. 32, no. 2, pp. 99–108, 2007.

[3] W. Lu and C. M. Lieber, "Semiconductor nanowires," *J. Phys. D, Appl. Phys.*, vol. 39, no. 21, pp. R387–R406, Oct. 2006.

[4] A. M. Morales and C. M. Lieber, "A laser ablation method for the synthesis of crystalline semiconductor nanowires," *Science*, vol. 279, no. 5348, pp. 208–211, Jan. 1998.

[5] W. Lu, J. Xiang, B. P. Timko, Y. Wu, and C. M. Lieber, "One-dimensional hole gas in germanium/silicon nanowire heterostructures," in *Proc. Nat. Acad. Sci. USA*, Jul. 2005, vol. 102, pp. 10 046–10 051.

[6] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature*, vol. 441, no. 7092, pp. 489–493, May 2006.

[7] Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell, and C. M. Lieber, "Controlled growth and structures of molecular-scale silicon nanowires," *Nano Lett.*, vol. 4, no. 3, pp. 433–436, Feb. 2004.

[8] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 399–402, Feb. 1989.

[9] R. H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.

[10] C. Yang, Z. H. Zhong, and C. M. Lieber, "Encoding electronic properties by synthesis of axial modulation-doped silicon nanowires," *Science*, vol. 310, no. 5752, pp. 1304–1307, Nov. 2005.

[11] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, and C. M. Lieber, "Growth of nanowire superlattice structures for nanoscale photonics and electronics," *Nature*, vol. 415, no. 6872, pp. 617–620, Feb. 2002.

[12] Y. Cui, Z. H. Zhong, D. L. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, no. 2, pp. 149–152, Jan. 2003.

[13] G. F. Zheng, W. Lu, S. Jin, and C. M. Lieber, "Synthesis and fabrication of high-performance n-type silicon nanowire transistors," *Adv. Mater.*, vol. 16, no. 21, pp. 1890–1893, Sep. 2004.

[14] D. W. Wang, Q. Wang, A. Javey, R. Tu, H. J. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, "Germanium nanowire field-effect transistors with SiO_2 and high-κ HfO_2 gate dielectrics," *Appl. Phys. Lett.*, vol. 83, no. 12, pp. 2432–2434, Sep. 2003.

[15] X. Jiang, Q. Xiong, S. Nam, F. Qian, Y. Li, and C. M. Lieber, "InAs/InP radial nanowire heterostructures as high electron mobility devices," *Nano Lett.*, vol. 7, no. 10, pp. 3214–3218, Sep. 2007.

[16] Y. Li, J. Xiang, F. Qian, S. Gradecak, Y. Wu, H. Yan, D. A. Blom, and C. M. Lieber, "Dopant-free GaN/AlN/AlGaN radial nanowire heterostructures as high electron mobility transistors," *Nano Lett.*, vol. 6, no. 7, pp. 1468–1473, Jul. 2006.

[17] F. Qian, Y. Li, S. Gradecak, D. L. Wang, C. J. Barrelet, and C. M. Lieber, "Gallium nitride-based nanowire radial heterostructures for nanophotonics," *Nano Lett.*, vol. 4, no. 10, pp. 1975–1979, Sep. 2004.

[18] N. Wang, Y. F. Zhang, Y. H. Tang, C. S. Lee, and S. T. Lee, "SiO_2-enhanced synthesis of Si nanowires by laser ablation," *Appl. Phys. Lett.*, vol. 73, no. 26, pp. 3902–3904, Dec. 1998.

[19] R. S. Wagner, *Whisker Technology*. New York: Wiley, 1970.

[20] R. S. Wagner and W. C. Ellis, "Vapor–liquid–solid mechanism of single crystal growth," *Appl. Phys. Lett.*, vol. 4, no. 5, pp. 89–90, Mar. 1964.

[21] X. F. Duan, Y. Huang, Y. Cui, J. F. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, vol. 409, no. 6816, pp. 66–69, Jan. 2001.

[22] Y. Cui and C. M. Lieber, "Functional nanoscale electronic devices assembled using silicon nanowire building blocks," *Science*, vol. 291, no. 5505, pp. 851–853, Feb. 2001.

[23] Y. Huang, X. F. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science*, vol. 294, no. 5545, pp. 1313–1317, Nov. 2001.

[24] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. F. Wang, and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Appl. Phys. Lett.*, vol. 78, no. 15, pp. 2214–2216, Apr. 2001.

[25] J. Guo, J. Wang, E. Polizzi, S. Datta, and M. Lundstrom, "Electrostatics of nanowire transistors," *IEEE Trans. Nanotechnol.*, vol. 2, no. 4, pp. 329–334, Dec. 2003.

[26] Z. H. Chen, J. Appenzeller, J. Knoch, Y. M. Lin, and P. Avouris, "The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors," *Nano Lett.*, vol. 5, no. 7, pp. 1497–1502, Jul. 2005.

[27] Z. H. Zhong, Y. Fang, W. Lu, and C. M. Lieber, "Coherent single charge transport in molecular-scale silicon nanowires," *Nano Lett.*, vol. 5, no. 6, pp. 1143–1146, Jun. 2005.

[28] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.

[29] M. Shur, *Physics of Semiconductor Devices*. Englewood Cliffs, NJ: Prentice-Hall, 1990.

[30] D. A. Neamen, *Semiconductor Physics and Devices*. New York: McGraw-Hill, 1997.

[31] D. Whang, S. Jin, Y. Wu, and C. M. Lieber, "Large-scale hierarchical organization of nanowire arrays for integrated nanosystems," *Nano Lett.*, vol. 3, no. 9, pp. 1255–1259, Aug. 2003.

[32] H. Grabert and M. H. Devoret, *Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures*. New York: Plenum, 1992.

[33] T. Altebaeumer and H. Ahmed, "Tunnel barrier formation in silicon nanowires," *Jpn. J. Appl. Phys. 1, Regul. Rap. Short Notes*, vol. 42, no. 2A, pp. 414–417, 2003.

[34] A. Tilke, R. H. Blick, H. Lorenz, and J. P. Kotthaus, "Single-electron tunneling in highly doped silicon nanowires in a dual-gate configuration," *J. Appl. Phys.*, vol. 89, no. 12, pp. 8159–8162, Jun. 2001.

[35] A. B. Greytak, L. J. Lauhon, M. S. Gudiksen, and C. M. Lieber, "Growth and transport properties of complementary germanium nanowire field-effect transistors," *Appl. Phys. Lett.*, vol. 84, no. 21, pp. 4176–4178, May 2004.

[36] L. Zhang, R. Tu, and H. Dai, "Parallel core-shell metal–dielectric–semiconductor germanium nanowires for high-current surround-gate field-effect transistors," *Nano Lett.*, vol. 6, no. 12, pp. 2785–2789, Oct. 2006.

[37] M. T. Bjork, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg, and L. Samuelson, "One-dimensional steeplechase for electrons realized," *Nano Lett.*, vol. 2, no. 2, pp. 87–89, Jan. 2002.

[38] L. E. Jensen, M. T. Bjork, S. Jeppesen, A. I. Persson, B. J. Ohlsson, and L. Samuelson, "Role of surface diffusion in chemical beam epitaxy of InAs nanowires," *Nano Lett.*, vol. 4, no. 10, pp. 1961–1964, Sep. 2004.

[39] S. A. Dayeh, D. P. R. Aplin, X. T. Zhou, P. K. L. Yu, E. T. Yu, and D. L. Wang, "High electron mobility InAs nanowire field-effect transistors," *Small*, vol. 3, no. 2, pp. 326–332, 2007.

[40] C. Thelander, M. T. Bjork, M. W. Larsson, A. E. Hansen, L. R. Wallenberg, and L. Samuelson, "Electron transport in InAs nanowires and heterostructure nanowire devices," *Solid State Commun.*, vol. 131, no. 9/10, pp. 573–579, Sep. 2004.

[41] T. Bryllert, L. E. Wernersson, L. E. Froberg, and L. Samuelson, "Vertical high-mobility wrap-gated InAs nanowire transistor," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 323–325, May 2006.

[42] Y. C. Kong, D. P. Yu, B. Zhang, W. Fang, and S. Q. Feng, "Ultraviolet-emitting ZnO nanowires synthesized by a physical vapor deposition approach," *Appl. Phys. Lett.*, vol. 78, no. 4, pp. 407–409, Jan. 2001.

[43] Z. W. Pan, S. Dai, C. M. Rouleau, and D. H. Lowndes, "Germanium-catalyzed growth of zinc oxide nanowires: A semiconductor catalyst for nanowire synthesis," *Angew. Chem., Int. Ed. Engl.*, vol. 44, no. 2, pp. 274–278, Dec. 2005.

[44] M. Yang, G. S. Pang, L. F. Jiang, and S. H. Feng, "Hydrothermal synthesis of one-dimensional zinc oxides with different precursors," *Nanotechnology*, vol. 17, no. 1, pp. 206–212, Dec. 2006.
[45] W. I. Park, D. H. Kim, S. W. Jung, and G. C. Yi, "Metalorganic vapor-phase epitaxial growth of vertically well-aligned ZnO nanorods," *Appl. Phys. Lett.*, vol. 80, no. 22, pp. 4232–4234, Jun. 2002.
[46] S. W. Kim, S. Fujita, and S. Fujita, "ZnO nanowires with high aspect ratios grown by metalorganic chemical vapor deposition using gold nanoparticles," *Appl. Phys. Lett.*, vol. 86, no. 15, p. 153 119, Apr. 2005.
[47] Z. W. Liu, C. K. Ong, T. Yu, and Z. X. Shen, "Catalyst-free pulsed-laser-deposited ZnO nanorods and their room-temperature photoluminescence properties," *Appl. Phys. Lett.*, vol. 88, no. 5, p. 053 110, Jan. 2006.
[48] Y. W. Heo, V. Varadarajan, M. Kaufman, K. Kim, D. P. Norton, F. Ren, and P. H. Fleming, "Site-specific growth of ZnO nanorods using catalysis-driven molecular-beam epitaxy," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3046–3048, Oct. 2002.
[49] Z. R. Dai, Z. W. Pan, and Z. L. Wang, "Novel nanostructures of functional oxides synthesized by thermal evaporation," *Adv. Funct. Mater.*, vol. 13, no. 1, pp. 9–24, Jan. 2003.
[50] Q. Wan, E. Dattoli, and W. Lu, "Doping-dependent electrical characteristics of SnO_2 nanowires," *Small*, vol. 4, no. 4, pp. 451–454, Apr. 2008.
[51] Q. Wan, E. N. Dattoli, W. Y. Fung, W. Guo, Y. Chen, X. Pan, and W. Lu, "High-performance transparent conducting oxide nanowires," *Nano Lett.*, vol. 6, no. 12, pp. 2909–2915, Dec. 2006.
[52] Q. Wan, E. N. Dattoli, and W. Lu, "Transparent metallic Sb-doped SnO_2 nanowires," *Appl. Phys. Lett.*, vol. 90, no. 22, p. 222 107, May 2007.
[53] W. I. Park and G. C. Yi, "Electroluminescence in n-ZnO nanorod arrays vertically grown on p-GaN," *Adv. Mater.*, vol. 16, no. 1, pp. 87–90, Jan. 2004.
[54] H. Kind, H. Q. Yan, B. Messer, M. Law, and P. D. Yang, "Nanowire ultraviolet photodetectors and optical switches," *Adv. Mater.*, vol. 14, no. 2, pp. 158–160, Jan. 2002.
[55] K. Keem, H. Kim, G. T. Kim, J. S. Lee, B. Min, K. Cho, M. Y. Sung, and S. Kim, "Photocurrent in ZnO nanowires grown from Au electrodes," *Appl. Phys. Lett.*, vol. 84, no. 22, pp. 4376–4378, May 2004.
[56] M. S. Arnold, P. Avouris, Z. W. Pan, and Z. L. Wang, "Field-effect transistors based on single semiconducting oxide nanobelts," *J. Phys. Chem. B*, vol. 107, no. 3, pp. 659–663, 2003.
[57] W. I. Park, J. S. Kim, G. C. Yi, and H. J. Lee, "ZnO nanorod logic circuits," *Adv. Mater.*, vol. 17, no. 11, pp. 1393–1397, May 2005.
[58] E. N. Dattoli, Q. Wan, W. Guo, Y. Chen, X. Pan, and W. Lu, "Fully transparent thin-film transistor devices based on SnO_2 nanowires," *Nano Lett.*, vol. 7, no. 8, pp. 2463–2469, Aug. 2007.
[59] Q. Wan, Q. H. Li, Y. J. Chen, T. H. Wang, X. L. He, J. P. Li, and C. L. Lin, "Fabrication and ethanol sensing characteristics of ZnO nanowire gas sensors," *Appl. Phys. Lett.*, vol. 84, no. 18, pp. 3654–3656, May 2004.
[60] H. T. Wang, B. S. Kang, F. Ren, L. C. Tien, P. W. Sadik, D. P. Norton, S. J. Pearton, and J. Lin, "Hydrogen-selective sensing at room temperature with ZnO nanorods," *Appl. Phys. Lett.*, vol. 86, no. 24, p. 243 503, Jun. 2005.
[61] Z. Y. Fan and J. G. Lu, "Zinc oxide nanostructures: Synthesis and properties," *J. Nanosci. Nanotechnol.*, vol. 5, no. 10, pp. 1561–1573, Oct. 2005.
[62] Q. Wan, J. Huang, Z. Xie, T. Wang, E. N. Dattoli, and W. Lu, "Branched SnO_2 nanowires on metallic nanowire backbones for ethanol sensors application," *Appl. Phys. Lett.*, vol. 92, no. 10, p. 102 101, Mar. 2008.
[63] C. J. Lee, T. J. Lee, S. C. Lyu, Y. Zhang, H. Ruh, and H. J. Lee, "Field emission from well-aligned zinc oxide nanowires grown at low temperature," *Appl. Phys. Lett.*, vol. 81, no. 19, pp. 3648–3650, Nov. 2002.
[64] S. H. Jo, J. Y. Lao, Z. F. Ren, R. A. Farrer, T. Baldacchini, and J. T. Fourkas, "Field-emission studies on thin films of zinc oxide nanowires," *Appl. Phys. Lett.*, vol. 83, no. 23, pp. 4821–4823, Dec. 2003.
[65] Y. Wu, J. Xiang, C. Yang, W. Lu, and C. M. Lieber, "Single-crystal metallic nanowires and metal/semiconductor nanowire heterostructures," *Nature*, vol. 430, no. 6995, pp. 61–65, Jul. 2004.
[66] G. M. Cohen, M. J. Rooks, J. O. Chu, S. E. Laux, P. M. Solomon, J. A. Ott, R. J. Miller, and W. Haensch, "Nanowire metal–oxide–semiconductor field effect transistor with doped epitaxial contacts for source and drain," *Appl. Phys. Lett.*, vol. 90, no. 23, p. 233 110, Jun. 2007.
[67] L. J. Lauhon, M. S. Gudiksen, C. L. Wang, and C. M. Lieber, "Epitaxial core-shell and core-multishell nanowire heterostructures," *Nature*, vol. 420, no. 6911, pp. 57–61, Nov. 2002.
[68] C. Thelander, T. Martensson, M. T. Bjork, B. J. Ohlsson, M. W. Larsson, L. R. Wallenberg, and L. Samuelson, "Single-electron transistors in heterostructure nanowires," *Appl. Phys. Lett.*, vol. 83, no. 10, pp. 2052–2054, Sep. 2003.
[69] L. J. Lauhon, M. S. Gudiksen, and C. M. Lieber, "Semiconductor nanowire heterostructures," *Philos. Trans. R. Soc. Lond. Ser. A: Math. Phys. Sci.*, vol. 362, no. 1819, pp. 1247–1260, Jun. 2004.
[70] Y. Hu, J. Xiang, G. Liang, H. Yan, and C. M. Lieber, "Sub-100 nanometer channel length Ge/Si nanowire transistors with potential for 2 THz switching speed," *Nano Lett.*, vol. 8, no. 3, pp. 925–930, Mar. 2008.
[71] C. W. J. Beenakker and H. van Houten, *Solid State Physics: Advances in Research and Applications*. San Diego, CA: Academic, 1991.
[72] H. Sakaki, "Scattering suppression and high-mobility effect of size-quantized electrons in ultrafine semiconductor wire structures," *Jpn. J. Appl. Phys.*, vol. 19, pp. L735–L738, Dec. 1980.
[73] S. M. Cronenwett, H. J. Lynch, D. Goldhaber-Gordon, L. P. Kouwenhoven, C. M. Marcus, K. Hirose, N. S. Wingreen, and V. Umansky, "Low-temperature fate of the 0.7 structure in a point contact: A Kondo-like correlated state in an open system," *Phys. Rev. Lett.*, vol. 88, no. 22, p. 226 805, Jun. 2002.
[74] A. Kristensen, H. Bruus, A. E. Hansen, J. B. Jensen, P. E. Lindelof, C. J. Marckmann, J. Nygard, C. B. Sorensen, F. Beuscher, A. Forchel, and M. Michel, "Bias and temperature dependence of the 0.7 conductance anomaly in quantum point contacts," *Phys. Rev. B, Condens. Matter*, vol. 62, no. 16, pp. 10 950–10 957, Oct. 2000.
[75] S. Shapira, U. Sivan, P. M. Solomon, E. Buchstab, M. Tischler, and G. B. Yoseph, "Thermodynamics of a charged fermion layer at high rs values," *Phys. Rev. Lett.*, vol. 77, no. 15, pp. 3181–3184, Oct. 1996.
[76] A. Yacoby, H. L. Stormer, N. S. Wingreen, L. N. Pfeiffer, K. W. Baldwin, and K. W. West, "Nonuniversal conductance quantization in quantum wires," *Phys. Rev. Lett.*, vol. 77, no. 22, pp. 4612–4615, Nov. 1996.
[77] J. Xiang, A. Vidan, M. Tinkham, R. M. Westervelt, and C. M. Lieber, "Ge/Si nanowire mesoscopic Josephson junctions," *Nat. Nanotechnol.*, vol. 1, no. 3, pp. 208–213, Dec. 2006.
[78] M. Tinkham, *Introduction to Superconductivity*. New York: Dover, 1996.
[79] C. W. J. Beenakker and H. van Houten, "Josephson current through a superconducting quantum point contact shorter than the coherence length," *Phys. Rev. Lett.*, vol. 66, no. 23, pp. 3056–3059, Jun. 1991.
[80] M. Octavio, M. Tinkham, G. E. Blonder, and T. M. Klapwijk, "Subharmonic energy-gap structure in superconducting constrictions," *Phys. Rev. B, Condens. Matter*, vol. 27, no. 11, pp. 6739–6746, Jun. 1983.
[81] Y. Hu, H. O. H. Churchill, D. J. Reilly, J. Xiang, C. M. Lieber, and C. M. Marcus, "A Ge/Si heterostructure nanowire-based double quantum dot with integrated charge sensor," *Nat. Nanotechnol.*, vol. 2, no. 10, pp. 622–625, Oct. 2007.
[82] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking nanotechnology for high-performance and low-power logic transistor applications," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 153–158, Mar. 2005.
[83] J. Guo, A. Javey, H. J. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," in *IEDM Tech. Dig.*, 2004, pp. 703–706.
[84] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-kappa/metal-gate stack and its MOSFET characteristics," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 408–410, Jun. 2004.
[85] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[86] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, and H. Dai, "Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays," *Nano Lett.*, vol. 4, no. 7, pp. 1319–1322, Jun. 2004.
[87] I. Aberg, C. Ni Chleirigh, O. O. Olubuyide, X. Duan, and J. L. Hoyt, "High electron and hole mobility enhancements in thin-body strained Si/strained SiGe/strained Si heterostructures on insulator," in *IEDM Tech. Dig.*, 2004, pp. 173–176.
[88] A. E. A. Ritenour, "Epitaxial strained germanium p-MOSFETs with HfO_2 gate dielectric and TaN gate electrode," in *IEDM Tech. Dig.*, 2003, pp. 433–436.
[89] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1853–1864, Sep. 2003.
[90] G. C. Liang, J. Xiang, N. Kharche, G. Klimeck, C. M. Lieber, and M. Lundstrom, "Performance analysis of a Ge/Si core/shell nanowire field-effect transistor," *Nano Lett.*, vol. 7, no. 3, pp. 642–646, Feb. 2007.

[91] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III–V nitrides," *Phys. Rev. B, Condens. Matter*, vol. 56, no. 16, pp. R10 024–R10 027, Oct. 1997.
[92] F. Qian, S. Gradecak, Y. Li, C. Y. Wen, and C. M. Lieber, "Core/multishell nanowire heterostructures as multicolor, high-efficiency light-emitting diodes," *Nano Lett.*, vol. 5, no. 11, pp. 2287–2291, Nov. 2005.
[93] L. Shen, S. Heikman, B. Moran, R. Coffie, N. Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Lett.*, vol. 22, no. 10, pp. 457–459, Oct. 2001.
[94] J. H. Davies, *The Physics of Low-Dimensional Semiconductors: An Introduction*. Cambridge, U.K.: Cambridge Univ. Press, 1997.
[95] P. Ranade *et al.*, "High performance 35 nm L_{GATE} CMOS transistors featuring NiSi metal gate (FUSI), uniaxial strained silicon channels and 1.2 nm gate oxide," in *IEDM Tech. Dig.*, 2005, p. 217.
[96] B. Messer, J. H. Song, and P. D. Yang, "Microchannel networks for nanowire patterning," *J. Amer. Chem. Soc.*, vol. 122, pp. 10 232–10 233, 2000.
[97] Y. Huang, X. F. Duan, Q. Q. Wei, and C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science*, vol. 291, no. 5504, pp. 630–633, Jan. 2001.
[98] F. Kim, S. Kwan, J. Akana, and P. Yang, "Langmuir–Blodgett nanorod assembly," *J. Amer. Chem. Soc.*, vol. 123, no. 18, pp. 4360–4361, May 2001.
[99] A. Tao, F. Kim, C. Hess, J. Goldberger, R. He, Y. Sun, Y. Xia, and P. Yang, "Langmuir–Blodgett silver nanowire monolayers for molecular sensing using surface-enhanced Raman spectroscopy," *Nano Lett.*, vol. 3, no. 9, pp. 1229–1233, Aug. 2003.
[100] G. H. Yu, A. Y. Cao, and C. M. Lieber, "Large-area blown bubble films of aligned nanowires and carbon nanotubes," *Nat. Nanotechnol.*, vol. 2, no. 6, pp. 372–377, Jun. 2007.
[101] G. H. Yu, X. L. Li, C. M. Lieber, and A. Y. Cao, "Nanomaterial-incorporated blown bubble films for large-area, aligned nanostructures," *J. Mater. Chem.*, vol. 18, no. 7, pp. 728–734, 2008.
[102] A. Ulman, *An Introduction to Ultrathin Organic Films: From Langmuir–Blodgett to Self-Assembly*. New York: Academic, 1991.
[103] D. Whang, S. Jin, and C. M. Lieber, "Nanolithography using hierarchically assembled nanowire masks," *Nano Lett.*, vol. 3, no. 7, pp. 951–954, Jun. 2003.
[104] A. Javey, S.-W. Nam, R. S. Friedman, H. Yan, and C. M. Lieber, "Layer-by-layer assembly of nanowires for three-dimensional, multifunctional electronics," *Nano Lett.*, vol. 7, no. 3, pp. 773–777, Feb. 2007.
[105] Z. Fan, J. C. Ho, Z. A. Jacobson, R. Yerushalmi, R. L. Alley, H. Razavi, and A. Javey, "Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing," *Nano Lett.*, vol. 8, no. 1, pp. 20–25, 2008.
[106] M. S. Islam, S. Sharma, T. I. Kamins, and R. S. Williams, "Ultrahigh-density silicon nanobridges formed between two vertical silicon surfaces," *Nanotechnology*, vol. 15, no. 5, pp. L5–L8, 2004.
[107] D. G. R. He, R. Fan, I. Hochbaum, C. Carraro, R. Maboudian, and P. Yang, "Si nanowire bridges in microtrenches: Integration of growth into device fabrication," *Adv. Mater.*, vol. 17, no. 17, pp. 2098–2102, Apr. 2005.
[108] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nat. Nanotechnol.*, vol. 2, no. 4, pp. 230–236, Apr. 2007.
[109] J. Goldberger, A. I. Hochbaum, R. Fan, and P. Yang, "Silicon vertically integrated nanowire field effect transistors," *Nano Lett.*, vol. 6, no. 5, pp. 973–977, Mar. 2006.
[110] H. R. Volker Schmidt, S. Senz, S. Karg, W. Riess, and U. Göele, "Realization of a silicon nanowire vertical surround-gate field-effect transistor," *Small*, vol. 2, no. 1, pp. 85–88, 2006.
[111] M. T. Bjork, O. Hayden, H. Schmid, H. Riel, and W. Riess, "Vertical surround-gated silicon nanowire impact ionization field-effect transistors," *Appl. Phys. Lett.*, vol. 90, no. 14, p. 142 110, Apr. 2007.
[112] R. He and P. Yang, "Giant piezoresistance effect in silicon nanowires," *Nat. Nanotechnol.*, vol. 1, no. 1, pp. 42–46, Oct. 2006.
[113] X. L. Feng, R. He, P. Yang, and M. L. Roukes, "Very high frequency silicon nanowire electromechanical resonators," *Nano Lett.*, vol. 7, no. 7, pp. 1953–1959, Jun. 2007.
[114] P. J. Kuekes, D. R. Stewart, and R. S. Williams, "The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits," *J. Appl. Phys.*, vol. 97, no. 3, pp. 034 301-1–034 301-5, Feb. 2005.
[115] A. DeHon, "Array-based architecture for FET-based, nanoscale electronics," *IEEE Trans. Nanotechnol.*, vol. 2, no. 1, pp. 23–32, Mar. 2003.
[116] A. DeHon, P. Lincoln, and J. E. Savage, "Stochastic assembly of sublithographic nanoscale interfaces," *IEEE Trans. Nanotechnol.*, vol. 2, no. 3, pp. 165–174, Sep. 2003.
[117] Y. Chen, G. Y. Jung, D. A. A. Ohlberg, X. M. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, and R. S. Williams, "Nanoscale molecular-switch crossbar circuits," *Nanotechnology*, vol. 14, no. 4, pp. 462–468, Mar. 2003.
[118] D. B. Strukov and K. K. Likharev, "CMOL FPGA: A reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices," *Nanotechnology*, vol. 16, no. 6, pp. 888–900, Apr. 2005.
[119] D. B. Strukov and K. K. Likharev, "Prospects for terabit-scale nanoelectronic memories," *Nanotechnology*, vol. 16, no. 1, pp. 137–148, Jan. 2005.
[120] W. Lu and C. M. Lieber, "Nanoelectronics from the bottom up," *Nat. Mater.*, vol. 6, no. 11, pp. 841–850, Nov. 2007.
[121] J. R. Heath, P. J. Kuekes, G. S. Snider, and R. S. Williams, "A defect-tolerant computer architecture: Opportunities for nanotechnology," *Science*, vol. 280, no. 5370, pp. 1716–1721, Jun. 1998.
[122] Y. J. Dong, G. H. Yu, M. C. McAlpine, W. Lu, and C. M. Lieber, "Si/a-Si core/shell nanowires as nonvolatile crossbar switches," *Nano Lett.*, vol. 8, no. 2, pp. 386–391, Jan. 2008.
[123] M. Jafar and D. Haneman, "Switching in amorphous-silicon devices," *Phys. Rev. B, Condens. Matter*, vol. 49, no. 19, pp. 13611–13615, May 1994.
[124] S. H. Jo and W. Lu, "CMOS compatible nanoscale nonvolatile resistance switching memory," *Nano Lett.*, vol. 8, no. 2, pp. 392–397, Feb. 2008.
[125] P. J. Kuekes, W. Robinett, and R. S. Williams, "Improved voltage margins using linear error-correcting codes in resistor-logic demultiplexers for nanoelectronics," *Nanotechnology*, vol. 16, no. 9, pp. 1419–1432, Jun. 2005.
[126] J. C. Scott, "Is there an immortal memory?" *Science*, vol. 304, no. 5667, pp. 62–63, Apr. 2004.
[127] Z. H. Zhong, D. L. Wang, Y. Cui, M. W. Bockrath, and C. M. Lieber, "Nanowire crossbar arrays as address decoders for integrated nanosystems," *Science*, vol. 302, no. 5649, pp. 1377–1379, Nov. 2003.
[128] J. M. Shaw and P. F. Seidler, "Organic electronics: Introduction," *IBM J. Res. Develop.*, vol. 45, pp. 3–9, 2001.
[129] E. Lueder, *Liquid Crystal Displays: Addressing Schemes and Electro-Optical Effects*. Chichester, U.K.: Wiley, 2001.
[130] R. F. Service, "Electronics: New age semiconductors pick up the pace," *Science*, vol. 287, no. 5452, pp. 415–417, Jan. 2000.
[131] S. Uchikoga, "Low-temperature polycrystalline silicon thin-film transistor technologies for system-on-glass displays," *MRS Bull.*, vol. 27, no. 11, pp. 881–885, 2002.
[132] J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. Katz, K. Amundson, J. Ewing, and P. Drzaic, "Paper-like electronic displays: Large-area rubber-stamped plastic sheets of electronics and microencapsulated electrophoretic inks," *Proc. Nat. Acad. Sci. USA*, vol. 98, no. 9, pp. 4835–4840, Apr. 2001.
[133] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, "High-resolution inkjet printing of all-polymer transistor circuits," *Science*, vol. 290, no. 5499, pp. 2123–2126, Dec. 2000.
[134] M. C. McAlpine, R. S. Friedman, S. Jin, K. H. Lin, W. U. Wang, and C. M. Lieber, "High-performance nanowire electronics and photonics on glass and plastic substrates," *Nano Lett.*, vol. 3, no. 11, pp. 1531–1535, Oct. 2003.
[135] R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, and C. M. Lieber, "High-speed integrated nanowire circuits," *Nature*, vol. 434, p. 1085, Apr. 2005.
[136] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM J. Res. Develop.*, vol. 45, pp. 11–27, 2001.
[137] Y. Chen, J. An, P. Kazlas, A. Ritenour, H. Gates, and M. McMreary, "Electronic paper: Flexible active-matrix electronic ink display," *Nature*, vol. 423, no. 6936, p. 136, May 2003.
[138] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldman, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature*, vol. 425, no. 6955, pp. 274–278, Sep. 2003.
[139] J.-H. Ahn, H.-S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, and J. A. Rogers, "Heterogeneous three-dimensional electronics by use of printed semiconductor nanomaterials," *Science*, vol. 314, no. 5806, pp. 1754–1757, Dec. 2006.
[140] D.-H. Kim, J.-H. Ahn, W. M. Choi, H.-S. Kim, T.-H. Kim, J. Song, Y. Y. Huang, Z. Liu, C. Lu, and J. A. Rogers, "Stretchable and foldable

silicon integrated circuits," *Science*, vol. 320, no. 5875, pp. 507–511, Apr. 2008.
[141] E. N. Dattoli, K. H. Kim, and W. Lu, "Radio frequency transparent nanowire thin-film transistors," unpublished.
[142] M. Ofuji, K. Abe, H. Shimizu, N. Kaji, R. Hayashi, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Fast thin-film transistor circuits based on amorphous oxide semiconductor," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 273–275, Apr. 2007.
[143] W. Fix, A. Ullmann, J. Ficker, and W. Clemens, "Fast polymer integrated circuits," *Appl. Phys. Lett.*, vol. 81, no. 9, pp. 1735–1737, Aug. 2002.
[144] R. E. Presley, D. Hong, H. Q. Chiang, C. M. Hung, R. L. Hoffman, and J. F. Wager, "Transparent ring oscillator based on indium gallium oxide thin-film transistors," *Solid State Electron.*, vol. 50, no. 3, pp. 500–503, Mar. 2006.
[145] F. Patolsky, B. P. Timko, G. F. Zheng, and C. M. Lieber, "Nanowire-based nanoelectronic devices in the life sciences," *MRS Bull.*, vol. 32, no. 2, pp. 142–149, 2007.
[146] J. R. Maiolo, B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, H. A. Atwater, and N. S. Lewis, "High aspect ratio silicon wire array photoelectrochemical cells," *J. Amer. Chem. Soc.*, vol. 129, no. 41, pp. 12 346–12 347, Oct. 2007.
[147] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, and C. M. Lieber, "Coaxial silicon nanowires as solar cells and nanoelectronic power sources," *Nature*, vol. 449, no. 7164, pp. 885–890, Oct. 2007.

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