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Harvard Team Makes Programmable Logic from Nanowires

Nanowires made into logic tiles could be basis of low-power nanoprocessors

By NEIL SAVAGE / FEBRUARY 2011

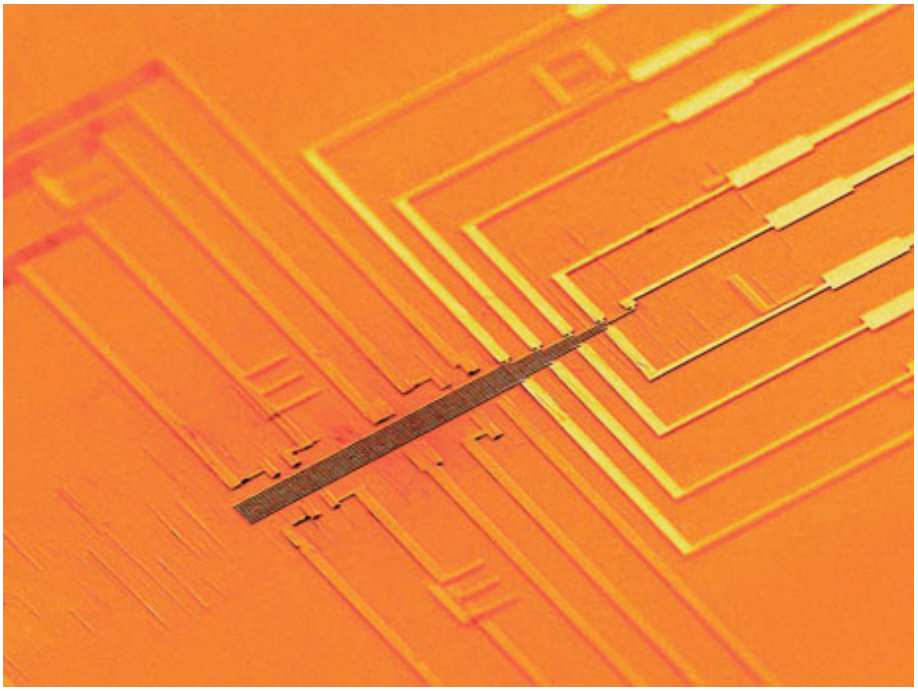

Photo: Lieber Group/Harvard University

9 February 2011—Transistors made from silicon-clad germanium nanowires—much smaller than traditional transistors—have for the first time been built into programmable "logic tiles," say researchers at Harvard University. Such tiles, layered together, could be the foundation for miniature processors that could control microrobots or run implantable medical monitors.

Professor Charles Lieber and his colleagues demonstrated silicon/germanium nanowire field-effect transistors (FETs) back in 2006; they were only 18 nanometers across and outperformed ordinary silicon FETs. But they were hard to manufacture with any consistency. "Researchers like myself like to say how good they are, but they just haven't been reproducible enough to assemble into larger circuits," Lieber says.

But Lieber's team reports in this week's *Nature* that they've been able to build a programmable array of nanowires that can have up to eight distinct logic gates. They dub such an array a "logic tile," with the idea that multiple tiles could be connected to perform more-complex logic functions.

The nanowires are made of a 10-nm-wide core of germanium, surrounded by a 2-nm-thick shell of silicon. The chief innovation was to cover those wires with a three-layer dielectric—first aluminum oxide, then zirconium oxide, then another layer of aluminum oxide. The three-layer material lets the wires trap charge carriers, allowing them to act as a nonvolatile memory, holding a positive or negative state even when no current is applied. The nanowires are laid out parallel to one another, with a source and drain on either end. A series of metal gate electrodes crosses the wires perpendicularly. Each nanowire contains multiple transistors, because each cross point between the nanowire and metal gate makes an individual transistor.

The design allows for many more transistors in a given area than traditional complementary metal-oxide-semiconductor (CMOS) manufacturing is likely to achieve. If CMOS reaches its limit at about 16 nm wide, as many researchers predict, CMOS transistors will still take up about eight times as much space as a nanowire transistor, says Lieber. Even so, he does not expect his technology to replace CMOS. "We can scale to very high densities, but we're not envisioning having

very high speed," he says. Lieber expects his transistors to operate at between 10 and 100 megahertz, instead of the gigahertz of CMOS. The flip side is that power demands will be much lower. While future CMOS is projected to use 10 to 100 nanowatts per transistor element, Lieber predicts his device will require only 1 nW per element. That would make it ideal for applications where the device is small and requires low power consumption and where fast processing is not needed. For instance, the tiles might make a controller for some microelectromechanical device, so it wouldn't need to be wired to a larger external processor. The tiles could run some sort of biosensor, to provide constant monitoring of a person's medical status.

The concept of using simpler arrays of transistors and building them up into a more complex processor—a "bottom up" approach—is one of the major innovations of nanotechnology, says Zhong Lin Wang, director of the Center for Nanostructure Characterization at Georgia Tech. The Lieber Research Group's nanoprocessor tile "represents a leap forward in the complexity and function of circuits built from the bottom up, and thus demonstrates that this bottom-up paradigm, which is distinct from the way commercial circuits are built today, can yield nanoprocessors and other integrated systems of the future," Wang says.

Lieber says the next challenge is to gain better control of the alignment of nanowires on the chip where they're placed, as well as reducing the small variations in the on-off voltage of individual wires. Once the researchers can make the tiles more uniform, they can link several of them together—a task Lieber expects to accomplish in the next year or two. He's hoping that the achievements his team has reported spark more interest in the technology, along with greater funding to move the project forward. "We're finally making some significant progress toward real nanoscale processors that we assemble from the bottom up," he says.

About the Author

Neil Savage writes about nanotech, optoelectronics, and other technology from Lowell, Mass. In February 2011, he reported on the development of a chip-scale MEMS Foucault Pendulum.