CHAPTER 1

Semiconductor Nanowire Growth and Integration

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1.1 Introduction

To date, numerous studies have been carried out to explore nanowires as new building blocks in electronics,[1–11] photonics,[12–24] solar-cells,[25–29] batteries,[30–34] nanogenerators,[35,36] and biological/chemical sensors.[37–44] Commonly cited properties of nanowires in these studies that can be advantageous are the small diameters, large surface area and smooth surfaces of the nanowire materials. For example, the large surface area and small diameters enabled nanowire electrodes to outperform thin-film electrodes in battery applications in terms of rate of charging/discharging and stability (*e.g.*, small diameters can better sustain strain without cracking), while the nearly-perfect material quality has enabled optical and electrical pumped nanowire lasers. Controlled nanowire growth has also enabled biosensors with integrated detectors and electrodes,[38,39,43] all achieved in a single nanowire during growth. Another aspect that sets the "bottom-up" nanowire system apart is the ability to obtain high quality nanowire heterostructures during

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growth, including core/shell radial heterostructures and superlattice axial heterostructures. Such heterostructures are extremely difficult if not impossible to obtain using conventional fabrication methods, while the small size and volumetric similarity of nanowire structures can produce coherently strained heterostructures free from interfacial dislocations even for materials with relatively large lattice mismatch (*e.g.*, Ge and Si). This ability to grow high-quality heterostructures has in turn led to the demonstration of several high-performance electrical and photonic devices that have only been demonstrated in the nanowire form.

This chapter will review fundamental growth topics for semiconductor nanowires, particularly focusing on the nanocluster-mediated VLS growth mechanism that has been widely employed and proven to be extremely flexible. The general concept of VLS growth will be introduced, followed by discussions of how the basic growth mode can be expanded to realize more complex and functional nanowire structures, such as radial and axial heterojunctions, as well as dopant incorporation. Factors affecting the growth dynamics and growth models will then be presented, followed by discussions of recent advances in increasing structural complexity, for example, through controlled formation of merged nanowires and kinks.

1.2 Basics of Nanocluster-Mediated VLS Nanowire Growth

Interest in nanowires was largely driven by the successful growths of 10 nm scale nanowires using the VLS method in the late 1990s.[45] The history of VLS growth can be traced back to the 1960s by Wagner,[46] who successfully employed this method to grow silicon microwires (whiskers). Whisker research remained a productive field; however, the relatively large size (>0.1 μm in diameter) of the whiskers produced in these early days offer few real practical advantages compared with fabricated structures. In fact, nanometer scale nanowires were not thought to be possible until the experimental demonstrations in 1998 by Morales *et al.*[45] The early demonstrations employed laser ablation to generate the source vapor needed for VLS growth to obtain single-crystalline Si and Ge nanowires. Soon the process was expanded to more controllable methods such as chemical deposition (CVD) and VLS, which has become the dominant option for nanowire growth due to its simple realization and flexible and excellent control over many aspects of the synthesis process. Figure 1.1 highlights some of the notable applications for nanowire devices.[45,47–49]

In a typical VLS growth process, as schematically illustrated in Figure 1.2, metal nanoparticles (either elemental particles such as Au, Ag, Cu, Al, Au or their alloys[50]) are employed as a catalyst to initiate and define nucleation, as well as facilitate activation/decomposition the molecular reactants (if used). During the growth process, the metal nanoparticles are first heated up above the eutectic temperature for the target metal–semiconductor system to create

a liquid metal–semiconductor eutectic alloy. With the presence of the semiconductor source material in its vapor phase, the eutectic alloy will continue to incorporate the semiconductor material through the vapor/liquid interface, ultimately resulting in supersaturation of the semiconductor material in the eutectic alloy. Further addition of the semiconductor source material into the eutectic alloy will eventually result in a nucleation event whereby the semiconductor material precipitates and creates a liquid/solid interface, which is also referred to as the growth interface. Nanowire growth is thus achieved *via* the transfer of the semiconductor material from the vapor source at the vapor/liquid interface into the eutectic, followed by continued solid addition at the liquid/solid interface. In this manner, the name VLS growth accurately captures the essence of the growth process from the starting vapor source stage to the final solid crystal stage. Notably, as growth continues, the metal catalyst will remain at the tip as the nanowire elongates below the liquid/solid interface, as schematically illustrated in Figure 1.2.[51]

The role of the metal nanoparticles is two-fold. Firstly, they are used to form the eutectic alloy with the target semiconductor, and in so doing also define the diameter of a growing nanowire. The phase diagram of the Au/Si eutectic system is shown in Figure 1.2, with a eutectic temperature of 363 °C with 19% Au in the alloy. This eutectic temperature is much lower than the melting temperature of either Au or Si so the VLS growth of Si nanowires can be carried out with Au catalysts in a low-temperature system. Low-temperature growth can be advantageous, for example, by excluding impurities that might otherwise be trapped in growing Si at higher temperatures. Secondly, the metal nanoparticles normally serve as a catalyst that promotes the decomposition of the semiconductor gaseous precursor, thus selectively producing the semiconductor source material at the targeted growth sites. In the case of Si nanowire growth, SiH_4 and Au are normally used as the precursor and catalysts, although other precursors such as Si_2H_6, SiH_2Cl_2, and $SiCl_4$ have also been employed.[50] The Au catalysts facilitate the decomposition of the precursor (*e.g.*, SiH_4 into Si and H_2) near the growth sites, as the Si atoms in turn incorporate into the Au nanoparticles to form the Au/Si eutectic alloy and eventually lead to VLS Si nanowire growth with Si atoms precipitated at the liquid/solid interface.

The use of metals such as Au can raise concerns regarding catalyst metal contamination during VLS growth. For example, Au is known to produce deep level traps in silicon and the existence of such deep level traps can be detrimental to the performance of nanowire-based electronics, in particular in the form of potentially reduced minority carrier life time and increased generation–recombination rates. With high angle annular dark field scanning transmission electron microscopy, Allen *et al.* were able to map out the Au locations in VLS grown Si nanowires.[52] It was found that Au is present in nanowires with a concentration exceeding the bulk solubility. The lack of concentration gradient along the nanowire also suggests incorporation during the growth to be the dominant process rather than post growth diffusion. However, electron beam induced current microscopy in the same

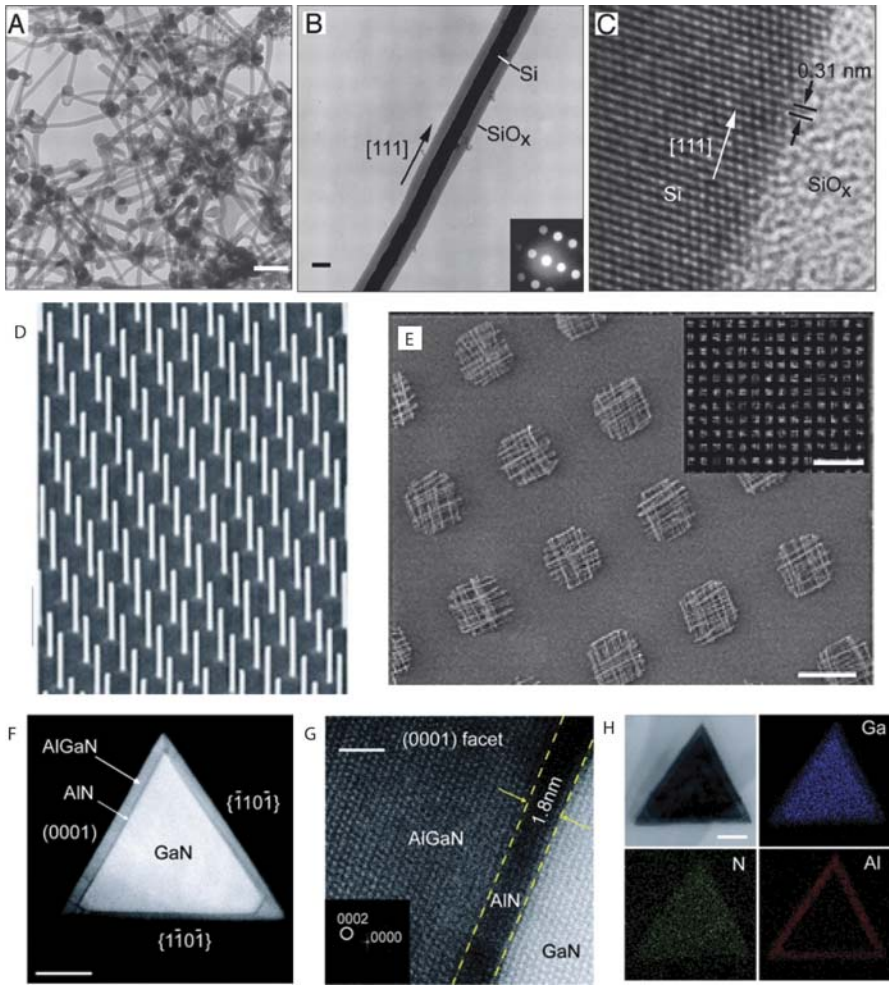

Figure 1.1 Overview of semiconductor nanowires and their applications. (A) TEM image of Si nanowires produced after ablation of a $Si_{0.9}Fe_{0.1}$ target. Scale bar: 100 nm. (B) Diffraction contrast TEM image of a Si nanowire. Crystalline material (the Si core) appears darker than amorphous material (SiO_x sheath) in this imaging mode. Scale bar: 10 nm. Inset: electron diffraction pattern recorded along the [211] zone axis perpendicular to the nanowire growth axis. (C) HRTEM image of the crystalline Si core and amorphous SiO_x sheath. The (111) planes (black arrows) (spacing 0.31 nm) are oriented perpendicular to the growth direction (white arrow). Reproduced with permission from ref. 45. Copyright (1998) American Association for the Advance of Science. (D) Tilted SEM image of a vertical InAs nanowire array grown on an InAs (111) B substrate. The spacing between nanowires is 0.5 μm. Reproduced with permission from ref. 47. Copyright (2004) American Chemical Society. (E) SEM image of patterned crossed nanowire arrays. Scale bar: 10 μm. Inset: large area dark field optical microscopy image of the crossed arrays. Scale bar: 100 μm.

study revealed that the minority carrier diffusion length in Si nanowires is mainly limited by the surface properties, not the bulk Au impurities.[52] These results were reconfirmed by recent advances in atom probe tomography that allow quantitative tomographic reconstructions of nanowires by removing and measuring the time of flight of individual atoms with high precision. For example, Eichfeld *et al.* studied metal incorporation in Al catalyzed Si nanowires and revealed the presence of a high Al concentration in Si exceeding the bulk solubility.[53] The formation of Al clusters is also reported, suggesting that not all Al are electrically active in Si nanowire and the unusually high Al composition may be explained by the presence of these non-equilibrium defects. On the other hand, a study performed on Au catalyzed Ge nanowires showed that no Au concentration is less than 0.2×10^{18} cm^{-3}, bonded by the detection limit of the experiment equipment,[54] indicating that metal incorporation may depend heavily on the growth condition and/or the material.

VLS nanowire growth is typically conducted in a chemical vapor deposition (CVD) chamber (including conventional hot-wall CVD, lamp-heated cold-wall CVD and metal–organic CVD (MOCVD) systems) where the precursor materials are introduced in the vapor phase and decompositions and nanowire growth take place at controlled temperatures and pressures. However, momentum and energy transfer methods such as pulsed laser ablation (PLA)[45] or molecular beam epitaxy (MBE)[55] can also be used to produce the vapor phase growth materials from solid targets, and VLS growth of nanowires using MBE and PLA has also been widely studied. The flexibility of the VLS method enabled it to be used for the growth of a broad range of nanowire materials other than Si, covering other group IV materials such as Ge,[56] group III–V (GaAs,[57] GaP,[16] InAs,[58] InP,[59] *etc.*), II–VI materials (ZnS,[60] ZnSe,[61] CdS,[62] *etc.*) and nitrides.[63] This level of flexibility makes VLS the predominant growth method for semiconductor nanowire growth. In the case of compound material nanowires, the semiconductor reactants are usually provided by metal–organic chemical vapor deposition (MOCVD)[64] or PLA.[65]

In a typical VLS–CVD process, the size of the nanowire is to a large extent determined by the size of the catalyst used. Wu *et al.* systematically studied the size distribution of Si nanowires synthesized using SiH_4/H_2 and Au nanoclusters *via* the VLS method in well controlled conditions.[66]

Reproduced with permission from ref. 49. Copyright (2003) American Chemical Society. (F) High-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of the cross section of a GaN/AlN/AlGaN nanowire. Scale bar: 50 nm. (G) Lattice-resolved HAADF-STEM image recorded at the (0001) facet of the nanowire. Dashed lines highlight the heterointerfaces between layers. Scale bar: 2 nm. (H) bright field STEM image and corresponding EDS elemental mapping of the same nanowire, indicating spatial distribution of Ga (blue), Al (red) and N (green), recorded on a GaN/AlN/AlGaN nanowire cross section. Scale bar: 50 nm. Reproduced with permission from ref. 48. Copyright (2006) American Chemical Society.

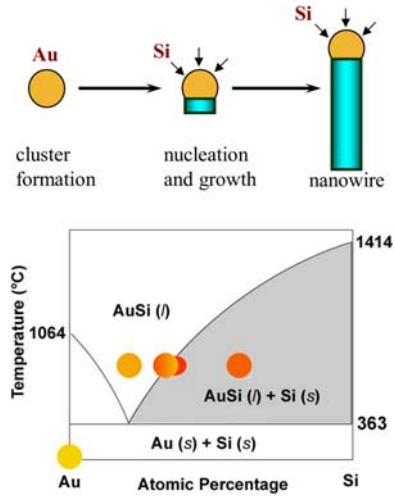

Figure 1.2 Schematic of VLS growth of Si nanowires. (Top) A liquid alloy droplet of AuSi is first formed above the eutectic temperature (363 °C) of Au and Si. Continued feeding of Si in the vapor phase into the liquid alloy causes oversaturation, resulting in nucleation and directional nanowire growth. (Bottom) Binary phase diagram for the AuSi system. Reproduced with permission from ref. 51.

High-resolution transmission electron microscopy (HRTEM) was used to examine these Si nanowires and revealed that the nanowires are single-crystalline even with diameters down to 3 nm. The nanowires showed narrow size distributions of 13.2 ± 1.7, 5.9 ± 1.1 and 4.6 ± 1.2 nm for Au nanoclusters of diameters of 10 (9.7 ± 1.5), 5 (4.9 ± 0.7) and 2 nm (3.3 ± 1 nm), respectively. The sizes of the nanowires are consistently slightly larger than those of the catalyst used, which can be explained by the supersaturation of Si in Au, which leads to the expansion of the eutectic alloy volume compared to the starting pure Au nanoparticle. Similar effects have also been reported in other VLS nanowire systems and verified through *in situ* imaging methods.[67] The excellent size control offered by VLS growth mediated with metal nanoparticles, which are commercially available at different specific diameters, is a significant advantage over other methods such as laser ablation or thermal annealing of a thin metal film, and has become the dominating method of choice – uniform nanowires with diameter down to a few nanometers can now be reliably obtained in a controlled fashion.

1.3 Nanowire Growth Dynamics

Considering that most nanowires synthesized through the VLS method are grown at near-equilibrium conditions, the growth processes can be considered primarily thermodynamically driven. As a result, the preferred growth mode (*e.g.*, nanowire growth direction) will be the one that minimizes the

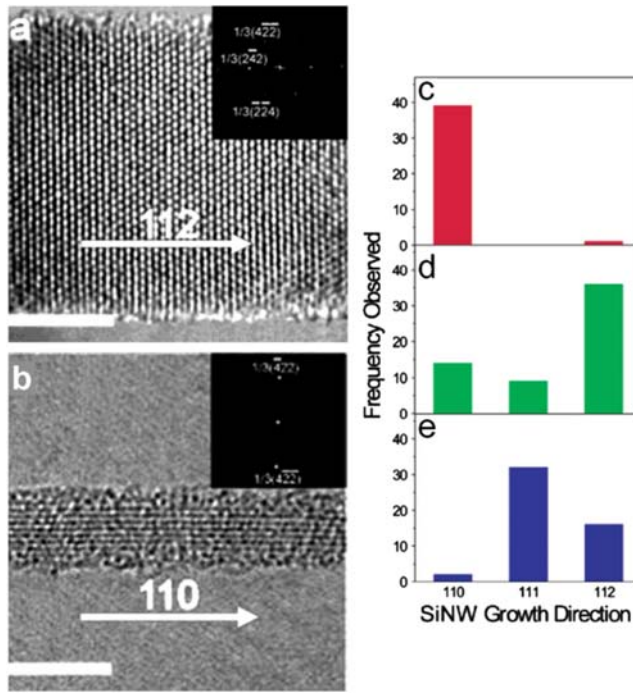

Figure 1.3 (a and b) HRTEM images of SiNWs with diameters of 12.3 (a) and 3.5 nm (b). Sale bar: 5 nm. (c–e) Histogram of the growth directions for SiNWs with diameters from 3 to 10 (c), 10 to 20 (d), and 20 to 30 nm (e). Reproduced with permission from ref. 66. Copyright (2004) American Chemical Society.

total free energy. However, kinetic effects dictate the process rates of the various steps involved in nanowire growth and can also play a key role during growth and affect the overall nanowire quality and growth dynamics.

From a thermodynamic point of view, the total free energy of the nanowire system includes the 'bulk' energy of the nanowire, the catalyst/nanowire (liquid/solid) interface energy, and the nanowire/vacuum (solid/vapor) interface energy. Given that the interface energies depend on the interface direction, one consequence of the thermodynamic driven VLS process is that a preferred growth direction can typically be obtained during VLS nanowire growth. Still taking the Si nanowire growth as an example, in Wu's study,[66] the growth directions of the Si nanowires with different diameters were examined in great detail *via* HRTEM. The results are summarized in the histogram in Figure 1.3. Earlier work on micrometer-scale, VLS grown Si whiskers showed a dominant preference along the ⟨111⟩ direction, which is believed to be determined by the formation of a single lowest-free-energy solid/liquid interface parallel to a single (111) plane.[46] This observation was confirmed by Wu *et al.* in nanowires with diameters larger than 20 nm.

However, for nanowires with diameters between 3 nm and 10 nm, the majority were found to grow along the ⟨110⟩ direction. Closer HRTEM analysis revealed that the Au/Si interface is composed of two V-shaped (111) planes, instead of a single (111) plane observed in larger nanowires (Figure 1.4). These results can be explained by the increasing contribution from the Si/vacuum surface energy to the total free energy as smaller nanowires have higher surface to volume ratios. The Si/vacuum surfaces parallel to ⟨110⟩ nanowires consist of (111) and (100) planes, which have lower free energies than the (110) surface planes found in ⟨111⟩ nanowires (Figure 1.4). This explains why growth along the ⟨110⟩ direction becomes more preferred as the diameter of the nanowires decreases. Growth along the ⟨112⟩ direction was also observed and was more commonly found in the diameter range between 10 and 20 nm and can be regarded as the transitional growth orientation since (112) plane is a stepped plane between (111) and (110) planes.

The understanding and subsequent control of the preferred growth directions in turn allow the design and growth of epitaxial nanowire structures. While VLS growth on an amorphous substrate such as SiO_2 results in

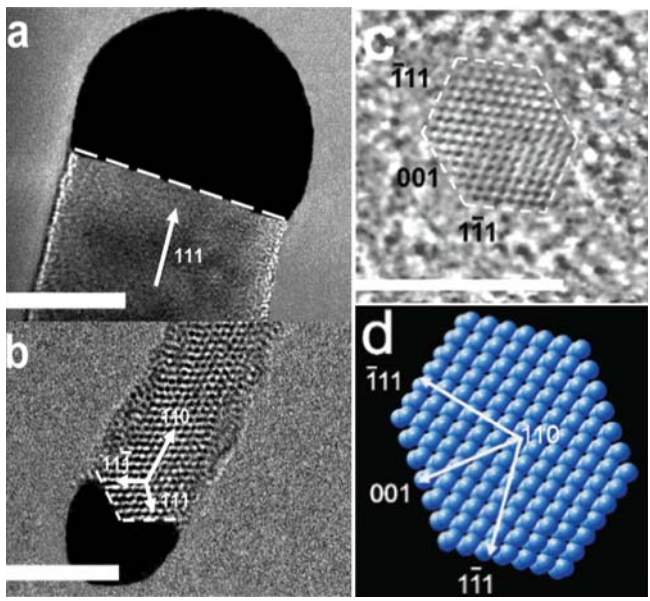

Figure 1.4 (a) HRTEM image of the catalyst alloy/NW interface of a SiNW showing ⟨111⟩ growth direction. Scale bar: 20 nm. (b) HRTEM image of a catalyst alloy/NW interface of a SiNW showing ⟨110⟩ growth direction. Scale bar: 5 nm. (c) HRTEM cross-sectional image (scale bar: 5 nm), and (d) equilibrium shapes for the NW cross section predicted from density functional theory calculation. Reproduced with permission from ref. 66. Copyright (2004) American Chemical Society.

nanowires with random directions, epitaxial growth can occur with crystalline substrates. For example, Jagannathan *et al.* observed that Ge nanowires grew predominately along the ⟨111⟩ direction on crystalline Si substrates. Interestingly, epitaxial ⟨111⟩ Ge nanowire growth was always obtained regardless of the orientation of the Si substrate.[68] For example, with a (111) substrate, most of the Ge wires will be vertical, while with a (100) or a (110) substrate the Ge nanowires will instead grow at a tilted angle to maintain the ⟨111⟩ growth direction. Similar to the CVD of thin films, high vacuum is generally a key to achieve good epitaxy, as the formation of an interfacial native oxide layer will hinder the process and cause degraded yield. By adding HF into the Au colloid and transferring the sample immediately to the CVD camber after catalyst dispersion, native oxide formation can be suppressed and high vertical growth yield can be obtained on (111) Si substrates (Figure 1.5).[56] A high-resolution TEM study confirmed the epitaxial relation between the nanowires and the substrate (Figure 1.5). The amorphous defect present at the interface has a lower *Z* contrast, which is likely a thin oxide layer prior to the growth.[68] Notably, a clear epitaxial relationship between the Ge nanowire and the Si substrate can be observed, despite the large (4.2%) lattice mismatch between the two materials. The high quality of the Si/Ge interface obtained during epitaxial nanowire growth was also recently verified through electrical characterizations.[69] A simple device structure such as p-Ge nanowire/n-Si substrate diode was fabricated and measured to examine the interface quality. Figure 1.5 presents the current–voltage (*I–V*) characteristics of a diode consisting of a p-type Ge nanowire grown on an n-type Si substrate, showing a nearly ideal diode behavior with an ideality factor of 1.16 at room temperature, and suggesting a very clean Ge/Si interface with low defect densities. For the epitaxial growth of Si nanowires, the use of a Cl-based precursor was found to help improve the vertical yield. Hochbaum *et al.* reported that gaseous HCl, a byproduct of $SiCl_4$ decomposition, is

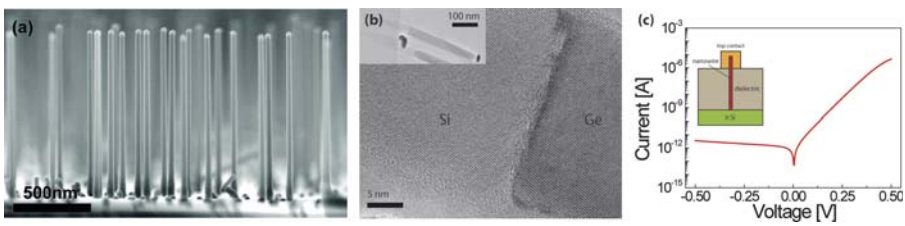

Figure 1.5 (a) Cross-section SEM image of GeNWs grown epitaxially on a (111) Si substrate showing predominantly vertically oriented GeNWs with uniform diameter and length. Reproduced with permission from ref. 56. Copyright (2007) American Chemical Society. (b) HRTEM of the Si/Ge interface grown using a similar method. (c) Typical *I–V* characteristic of a vertical nanowire Ge/Si P/N heterostructure diode with an ideality factor of 1.16. Reproduced with permission from ref. 69. Copyright (2013) American Chemical Society.

responsible for *in situ* etching of the oxide layer on the substrate surface and promoting epitaxial growth, while other precursors, such as SiH_4 alone without separately adding HCl gas, will not yield vertical Si nanowires on a (111) Si substrate.[70]

The exact nanowire morphology depends on how the supersaturated material precipitates and solidifies to sustain the continuous nanowire growth. The precipitation requires a nucleation process and consumes energy. To better illustrate the discussion, a typical VLS process can be simplified as a three phase system with the supply (s), collector (c) and crystal (k) in the vapor, liquid and solid phase, respectively (Figure 1.6). The three phase boundary (TPB) is the perimeter encircling the growth front. The change in Gibbs free energy when nucleation occurs can be expressed as the difference of energy released from chemical potential and energy needed for the newly created interfaces. The free energy change for nucleation at the TPB can be written as the following:

$$\Delta G_{\mathrm{TPB}} = -n\Delta\mu_{\mathrm{sk}} + P_{\mathrm{ck}}h\sigma_{\mathrm{ck}} + P_{\mathrm{sk}}h\sigma_{\mathrm{sk}} \tag{1.1}$$

where $\Delta\mu_{\mathrm{sk}}$ is the chemical potential difference between the vapor (supply) and solid (crystal) phases, $P_{\mathrm{ck}}(P_{\mathrm{sk}})$ and $\sigma_{\mathrm{ck}}(\sigma_{\mathrm{sk}})$ are respectively the perimeter length and the interface energy of the collector/crystal (supply/crystal), n is the number of atoms nucleated and h is the growth height in this nucleation event. The second and third terms in eqn (1.1) are related to the edge energy at the TPB. At TPB, these two terms can be minimized by adjusting the shape and placement of the nucleus to lower ΔG_{TPB}. As a result, ΔG_{TPB} at the TPB will be the lowest compared to other potential nucleation sites, making the TPB the most preferable place for nucleation.[71] Once nucleation occurs, the newly generated nuclei will propagate along the liquid/solid interface to form a new layer (a ledge) of the semiconductor crystal. This process is then repeated, leading to the continued nanowire growth in a layer by layer fashion. This process is schematically illustrated in Figure 1.6.

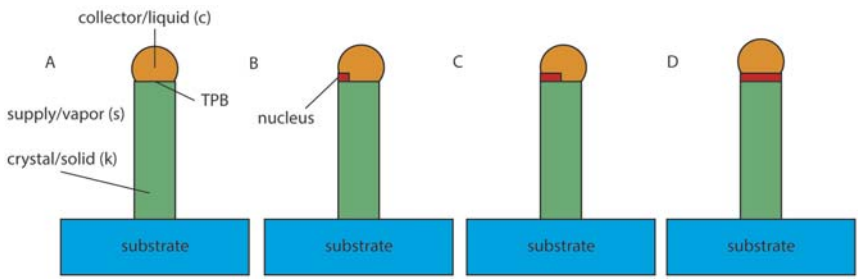

Figure 1.6 Schematic of the nanowire growth dynamics. (A) Different phases of the semiconductor material (*e.g.*, Si) during the nanowire growth. (B) Nucleation at the TPB. (C) Ledge propagation after nucleation. (D) Complete formation of one new layer. The process is then repeated.

The ledge formation and layer by layer growth were confirmed experimentally through *in situ* TEM studies by Hofmann *et al.* during Si nanowire growth using Pd as catalyst.[72] Figure 1.7 plots a few frames from a recorded video showing the ledge movement. Hofmann *et al.* also observed a negative correlation between the ledge height and the average propagation velocity, suggesting a nucleation limited process. Note that in Hofmann's study Pd and Si will form the Pd_2Si eutectic with a eutectic temperature of 810 °C. Since the experimental growth temperature is below this point, the eutectic alloy remains in solid form during the growth process and the growth occurs in the vapor–solid–solid (VSS) mode instead of the VLS mode. Similar results were also reported by Wen *et al.* for Au/Al assisted Si nanowire growth with *in situ* TEM at different temperatures.[73] While VSS growth below eutectic temperature showed slow ledge propagation and short incubation time (time between the formations of new ledges at TPB), VLS growth showed rapid ledge propagation and long incubation time. This difference can be understood from the low solubility of Si in the solid alloy. The energy barrier for nucleation requires the chemical potential (supersaturation) of Si in the alloy to be raised sufficiently high. In the VSS mode, a small amount of incoming Si from the vapor source is enough to cause sufficient superstation to enable the ledge formation, but the small amount of excess Si limits the ledge advancing velocity. On the other hand, the VLS mode leads to a much higher

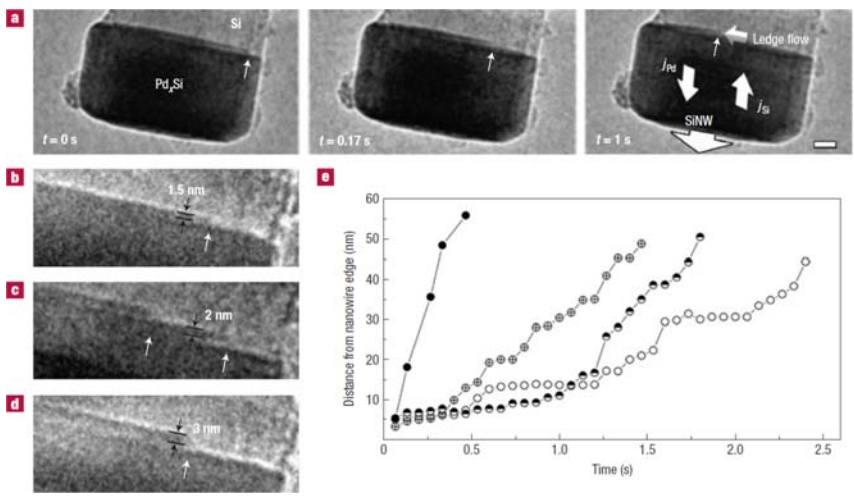

Figure 1.7 (a) Environmental TEM image sequences showing Si nanowire growth dynamics. The Si nanowires were grown inside a TEM chamber; *t* indicates elapsed time with respect to the first image. The ledge flow, growth direction and diffusion fluxes are shown schematically (b–d). Various ledge configurations at the Pd silicide/SiNW interface. (e) Measured step edge position *versus* time for four independent ledges of roughly equal approx 1.7 nm height in projection. Reproduced with permission from ref. 72. Copyright (2008) Nature Publishing Group.

Si concentration in the alloy, requiring more incoming Si atoms to reach the supersaturation for nucleation to occur. On the other hand, once nucleated, the large number of excess Si will drive the ledge to finish its advancing very rapidly.

Even though the fundamental nanowire growth process can be understood from thermodynamic arguments, the quality of the nanowire is strongly dependent on growth kinetics and can be affected by different growth parameters. There are two competing processes during VLS growth: (catalyst-mediated) precipitation through the liquid/solid interface, which leads to axial elongation, and (non-mediated) direct vapor deposition on the existing nanowire sidewall surface. The latter process results in radial thickening and eventually leads to tapering as the length of nanowires increases. Deposition of thin film on the substrate is also possible, if the growth condition permits. These processes are schematically illustrated in Figure 1.8.

Depending on the application, tapered nanowires are generally not preferable under most circumstances yet radial deposition will always be present and may even dominate if growth conditions such as temperature and pressure are not optimized. In the example of Si nanowire growth, since deposition on the radial direction is not catalyzed by metal particles and thus requires a much higher activation energy, radial deposition can be suppressed at low enough growth temperatures with the axial growth being the dominating process. Similarly, a cold-wall CVD system with local, rapid heating, as opposed to a hot-wall tube furnace reactor, can also be helpful to promote nanowire growth with minimal tapering.[2] Background gases such as H_2 have also been found to mitigate the radial growth by either suppressing the absorption of reactants through surface passivation[66] or by suppressing the dissociation of SiH_4.[74,75] H_2 has also been found to help reduce the surface roughness through passivation in a manner similar to that observed

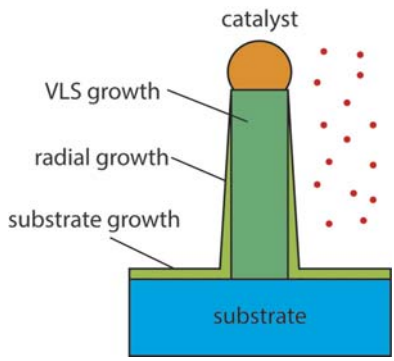

Figure 1.8 Possible deposition pathways in a VLS system. Depending on the growth parameters, VLS growth *via* catalyst alloy, radial overcoating on the existing nanowire sidewalls and thin film deposition on substrate may occur.

in thin-film growth.[76] Another route to reduce tapering is to introduce *in situ* etching chemistry to compensate for the radial overcoating. One such example is the use of gaseous HCl in InP nanowire growth to achieve straight sidewalls.[77]

Another growth kinetics related question is which process is rate-limiting during VLS growth. There are three candidates: (i) incorporation of the source material from the vapor into the liquid, (ii) diffusion through the liquid and (iii) incorporation from the liquid into the solid. With *in situ* TEM, Kodambaka *et al.* studied Au catalyzed Si nanowire growth with Si_2H_6 as the precursor, particularly focusing on the growth rate at different Si_2H_6 partial pressures and temperatures for nanowires with different diameters.[78] The results are summarized in Figure 1.9, from which a linear pressure dependent and diameter independent growth rate can be extracted, with an activation energy of 0.53 eV. In the absence of reverse processes (*i.e.*, evaporation of semiconductor species from the liquid to vapor), the nanowire growth rate is proportional to $P_{Si2H6}S$ under steady state, where P_{Si2H6} is the Si_2H_6 partial pressure and is directly related to the incoming flux and S is the sticking probability measuring the percentage of the molecules from the incoming flux that actually become incorporated into the alloy. Note that process (ii) and (iii) can affect the growth rate if and only if the sticking probability or evaporation rate depends on the chemical potential of Si in the alloy. Conversely, growth rate will affect the Si chemical potential *via* process (ii) and (iii). Thus, the observed linear relation between growth rate and Si_2H_6 partial pressure as shown in Figure 1.9 excludes these processes as the rate limiting factor under these particular experimental conditions, suggesting that the dissociative adsorption of the precursor on the alloy surface determines the growth rate instead.

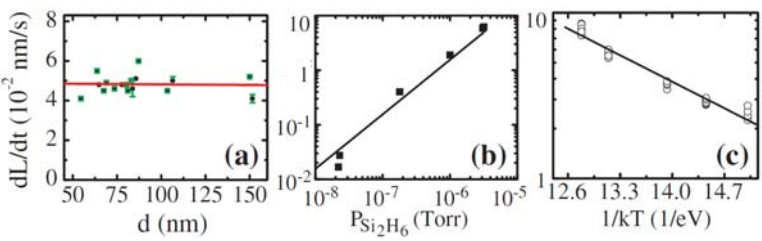

Figure 1.9 (a) The growth rate dL/dt *versus* the nanowire diameter d measured from an ensemble of Si nanowires. The solid line is a least-squares fit. (b) log–log plot of dL/dt of one particular nanowire grown at different precursor (Si_2H_6) partial pressures at a fixed temperature $T = 575$ °C. The solid line is the best (least-squares) fit of slope 1. (c) Arrhenius plot of dL/dt *versus* T for 28 nanowires at $P_{Si_2H_6} = 1 \times 10^{-6}$ Torr. Each data point represents an individual wire. The straight line is the least-squares fit; the activation energy is 0.53 ± 0.02 eV. Reproduced with permission from ref. 78. Copyright (2006) American Physical Society (http://journals.aps.org/prl/abstract/10.1103/PhysRevLett.96.096105).

Although VLS growth in general requires a growth temperature above the eutectic temperature for alloy formation, nanowire growth can in fact occur below this critical temperature,[79] although the exact state of the catalyst requires careful examination. For example, Kodambaka *et al.* studied the growth of Ge nanowires with Au catalyst nanoparticles using *in situ* TEM and found that both VLS and VSS growth can happen at the same temperature, and that the state of the catalyst depends on the growth pressure and the thermal history.[79] In one experimental condition, after an initial VLS growth at 335 °C, the Au catalyst did not solidify until the temperature drops to 235 °C, which is way below the eutectic temperature of 361 °C for the Ge/Au system. This effect was attributed to the inhabitation of Au nucleation from the Ge supersaturation so that the Au/Ge alloy remains in a supercooled liquid state and VLS growth still dominates even at this low temperature. The authors also observed that smaller alloys solidified sooner, indicating that the Gibbs–Thomson effect or other size-related effects are not the cause as otherwise the opposite trend should be seen. In addition, the VSS growth rate was found to be 10 to 100 times slower than VLS growth rate at the same temperature and pressure, preassembly as a result of the weaker surface reactivity and/or lower diffusivity through the solid in VSS growth.[79]

For certain materials the crystal structure can also be affected by the synthesis conditions. For example, most III–V materials in bulk crystallize in the cubic zinc blende (ZB) structure, while a mixture of ZB and wurtzite (WZ) structures can be found in the nanowire form.[80] The mix of ZB and WZ structures during III–V nanowire growth is believed to be a result of the layer by layer growth fashion. With the stacking sequence of ZB being abcabc and that of WZ being abab where each of the letters represents one of the three possible packing orders, one misplaced stacking layer *c* can result in a structural change. The ZB–WZ polytypism observed in the nanowire form in contrast to a dominate bulk ZB structure indicates that the WZ structure can (or must) possess low-energy surfaces so that the structural equilibrium may change when the surface to volume ratio is high.[80] For example, Dick *et al.* performed a detailed study on InAs nanowire growth *via* MOCVD with trimethylindium (TMIn) and arsine (AsH_3) catalyzed by gold aerosol particles, and found that the switch between the ZB crystal structure and the WZ structure is affected by temperature, V : III ratio and total precursor flow.[80] The effect of the changes in process parameters is complex and a quantitative conclusion is hard to draw. However, one important observation is that the process window for the dominant structure is quite narrow, indicating the decisive factor is thermodynamics rather than kinetics.[80] A possible explanation is that the changes in nucleation energy or facet surface energy shift the balance between WZ and ZB, thus making one structure more energetically favorable. It was found that the threshold temperature is 400 °C, below which pure ZB is achievable with appropriate V : III ratios while pure WZ can be obtained otherwise. Dick *et al.* also demonstrated that by abruptly changing the V : III ratio thin layer nanowire segments with opposite crystal structures can be obtained, making precise engineering of structure at the

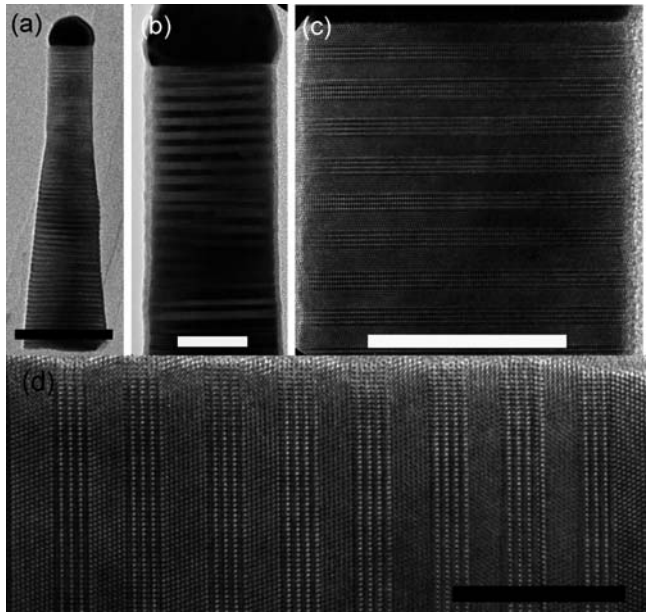

Figure 1.10 TEM images of InAs nanowire superlattices, defined by 60 periods of alternating ZB and WZ structures (each eight bilayers thick), viewed along the [110] zone axis. The nanowires were grown at 380 °C with WZ segments being formed during growth interrupts under group V precursor flow. (a) Full-length nanowire with alternating segments showing up as striped contrast. (b) Higher-magnification image showing the regular length of the striped segments; scale bar: 20 nm. (c) High-resolution image highlighting different crystal structures; scale bar: 20 nm. (d) High-resolution image showing the different positions of atom columns in ZB and WZ structures; scale bar: 10 nm. Reproduced with permission from ref. 81. Copyright (2010) American Chemical Society.

atomic level possible.[81] Figure 1.10 illustrates the superlattice formed in an InAs nanowire with alternating ZB and WZ structures (each segment eight bilayers thick). Importantly, the growth parameters, *e.g.*, temperature, V : III ratio and gas flow, have an interdependent effect on the preferable nanowire structure and the surface (edge) energies relevant to III–V nanowires are generally unknown, making it difficult to predict the growth results at certain growth conditions in general.

1.4 Nanowire Heterostructures

The VLS process can be readily adopted to create atomically sharp heterostructures in a controlled fashion. There are two main categories of nanowire heterostructures: axial heterostructures, where segments of nanowires

consist of different materials but have the same diameter, and radial heterostructures in the form of core/shell or core/multi-shell structures. Figure 1.11 shows schematically how axial and radial heterostructures can be formed during VLS growth. Heterostructure formation usually involves switching growing species by changing precursors during the growth. Depending on the target material, other parameters such as temperature and pressure may also be adjusted. Both axial and radial heterojunction formations have their unique advantages and applications, and have been demonstrated in VLS grown nanowires in several studies.[6,16,82–84]

Similar to the tapering issue discussed earlier, two competing deposition processes are always present during VLS heterostructure growth, *i.e.*, decomposition/deposition at the vapor/solid interface of the exposed nanowire sidewalls and the precipitation at the liquid/solid interface of the nanowire growth front. The relative growth rates of these two processes determine whether axial or radial heterostructure will be created: a radial heterostructure will be formed if the sidewall deposition dominates (Figure 1.11f), while an axial heterostructure can be obtained if reactants are exclusively deposited through the liquid/solid interface (Figure 1.11e). Notably, superlattice in the form of the axial heterostructure can be created by repetitive switching between different precursor materials.[16,82] While a radial superlattice is also achievable in principle, the core/multiple-shell structure is more commonly used.[83,84] Since the shell growth is very similar to planar thin film deposition, it can readily lead to radial hetero-epitaxy on the crystalline nanowire backbone.[51]

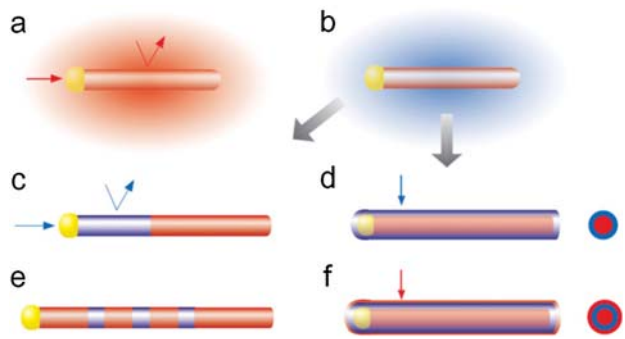

Figure 1.11 Schematic of nanowire heterostructure synthesis. (a) Preferential reactant incorporation at the catalyst (growth end) leads to one-dimensional axial growth. (b) A change in the reactant leads to either (c) axial heterostructure growth or (d) radial heterostructure growth depending on whether the reactant is preferentially incorporated (c) at the catalyst or (d) uniformly on the wire surface. Alternating reactants will produce (e) axial superlattices or (f) core/shell structures. Reproduced with permission from ref. 51.

1.4.1 Radial Nanowire Heterostructure

Radial core/shell heterostructure can be achieved if the preferable process is the decomposition/deposition on the grown nanowire surface, as schematically illustrated in Figure 1.11(f). Compared to a homogeneous nanowire, a core/shell nanowire heterostructure can be tailored through band structure engineering to provide better electrical and optical properties. For example, similar to the formation of two-dimensional electron[85] and hole[86] gases in high-electron mobility transistors (HEMTs), one-dimensional electron and hole gases can be obtained in core/shell nanowires by choosing the core and shell materials with appropriate band alignment. Lu *et al.* reported the existence of a one-dimensional hole gas in Ge/Si core/shell nanowires (Figure 1.12).[6] With a thin Si shell grown epitaxially around a Ge core, the large valence band offset of *ca.* 500 meV between Ge and Si at the interface provides quantum confinement that leads to the accumulation of free holes in the Ge core channel when the Fermi level lies below the valence band of Ge core. As a result, a Ge/Si core/shell nanowire will act as if it is heavily p-type doped even though both materials are not intentionally doped during the growth. Without dopants, which behave as scattering centers, the carriers in

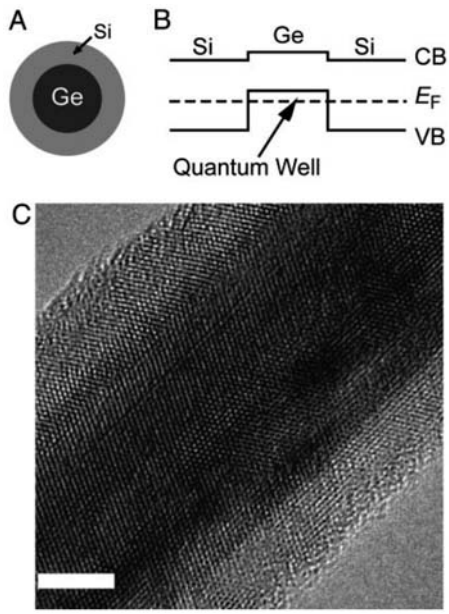

Figure 1.12 Ge/Si core/shell nanowires. (A) Schematic and (B) band diagram of the Ge/Si core/shell nanowire cross-section. The dashed line indicates the position of the Fermi level. (C) HRTEM image of a Ge/Si core/shell nanowire with a 15 nm diameter Ge (dark gray) core and a 5 nm Si (light gray) shell. Scale bar: 5 nm. Reproduced with permission from ref. 6.

the Ge core exhibit a long mean free path and high mobility, making them ideally suited for applications such as high performance nanowire transistors[6] and low-temperature quantum electronics.[6,87–90]

Following the same principle, other material combinations have been demonstrated in core/shell nanowire configuration. For example, GaN/InGaN/GaN, core/multi-shell nanowires were grown *via* MOCVD for high-efficiency light-emitting diode (LED) applications.[84] Multi-quantum well structures such as n-GaN/$In_xGa_{1-x}N$/GaN/p-AlGaN/p-GaN have also been demonstrated in core/multi-shell nanowire configurations.[83] The ability to define the dimension, doping level and material composition of individual layers in the nanowire heterostructures empowered researchers to design and fabricate nanoscale devices with great flexibility and precision that are not possible with homogeneous structures. For example, by varying the In composition from 1% to 35%, achieved by tuning the deposition temperature, a systematic redshift in the emission peak can be observed in forward bias electroluminescence (EL) measurements with increasing In composition for a n-GaN/$In_xGa_{1-x}N$/GaN/p-AlGaN/p-GaN nanowire with $In_xGa_{1-x}N$ band-edge emission (Figure 1.13). In addition, other nanostructures such as single-crystalline nanotubes can be obtained by using the core material as a sacrificial material. For example, silica nanotubes were obtained by growing Si/silica core/shell nanowire then selectively etching the Si core,[91] and single-crystalline Si nanotubes have been obtained by etching the Ge core in the Ge/Si core/shell nanowire structure.[92]

1.4.2 Axial Nanowire Heterostructure

During the synthesis of a radial nanowire heterostructure, the growth of the shell material is analogous to thin film deposition and does not involve reaction with the catalyst. On the other hand, the growth of an axial nanowire heterostructure requires continuation of the nanowire elongation process *via* the VLS process while the different vapor reactants are switched, all the while minimizing sidewall deposition. Thus, one prerequisite for the choice of catalyst material for axial nanowire heterostructure growth is its ability to promote reaction with at least two different gaseous precursors under the same or similar growth conditions. In the case of Si/Ge or Si/Si_xGe_{1-x} axial nanowire heterostructure, Au was found to meet this critical requirement and is often used to grow such nanowires. For example, Wu *et al.* demonstrated the fabrication of single-crystalline Si/SiGe axial nanowire heterostructures by introducing Ge vapor during growth through periodic laser pulsing of a solid Ge target into the gas mixture of $SiCl_4$ and H_2.[82] Pure Si segments can be obtained when the laser is off while the SiGe alloy segments will grow when the laser is turned on. Thus a Si/SiGe axial superlattice nanowire heterostructure is achieved. Figure 1.14a shows the SEM image and dark-field TEM image of the Si/SiGe axial nanowire heterostructure grown from laser pulse with periodicity of 30 s and duty cycle of 1/6. The SiGe segments show darker contrast due to the larger electron scattering cross

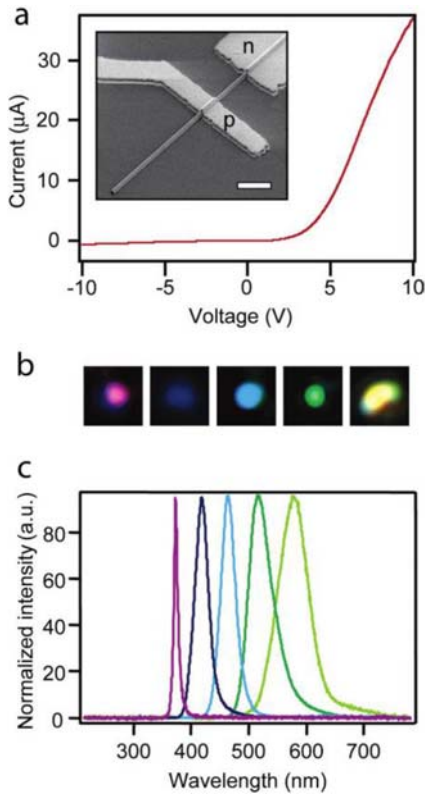

Figure 1.13 (a) Current *versus* voltage data recorded on a n-GaN/$In_xGa_{1-x}N$/GaN/p-AlGaN/p-GaN core/multi-shell (CMS) nanowire device. Inset: field emission scanning electron microscopy image of a representative device. Scale bar: 2 μm. (b) Optical microscopy images collected from the p-contact end of CMS nanowire LEDs with different In composition in forward bias, showing purple, blue, greenish-blue, green, and yellow emission, respectively. (c) Normalized EL spectra recorded from five representative forward-biased multicolor CMS nanowire LEDs. Reproduced with permission from ref. 83. Copyright (2005) American Chemical Society.

section of Ge atoms. The periodic Ge composition modulation is further confirmed *via* energy dispersive X-ray spectroscopy (EDS) results (Figure 1.14b). It is important to mention the structural parameters such as the composition of SiGe alloy, the periodicity of the superlattice and the lengths of individual segments are well controllable. For example, a more Ge rich alloy can be obtained by increasing the Ge/Si atom ratio *via* the laser intensity or reducing the SiH_4 flow rate. The periodicity of the superlattice can be adjusted by tuning the periodicity of the laser pulse and the growth rate of nanowire. Lastly, the length of each segment can be controlled by controlling the laser duty cycles.

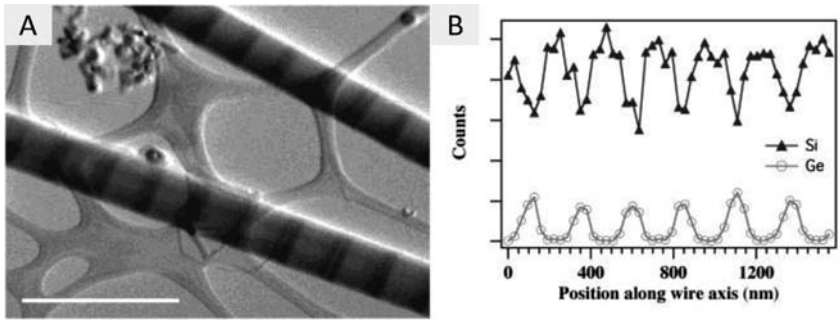

Figure 1.14 (A) STEM image of two Si/SiGe superlattice nanowires in bright field mode. Scale bar: 500 nm. (B) Line profile of EDS signals for Si and Ge components along the nanowire showing different Ge and Si compositions forming the superlattice. Reproduced with permission from ref. 82. Copyright (2002) American Chemical Society.

Similarly, GaP/GaAs superlattices have been grown by laser-assisted catalytic growth using GaAs and GaP targets.[16] The lengths of each segment were controlled by the number of pulses delivered to each target. Figure 1.15 shows a TEM image of a nanowire with three GaAs/GaP cycles. Elemental profiles of the same wire suggest well-defined segments without evident material intermixing. Photoluminescence measurement was also used to confirm the difference in the optoelectronic properties as GaAs (direct bandgap) gives strong luminescence and GaP (indirect bandgap) remains dark during the measurement.

An important parameter for nanowire heterostructures is the junction abruptness, which measures how fast the materials change across the heterojunction. Abrupt transition between two materials is critical for many applications, such as resonant tunneling diodes[93] and single electron transistors[4] where clearly defined tunnel barriers are essential for good device performance. However, axial nanowire heterostructures grown by the VLS method typically exhibit finite material gradients across the junction with relatively long leading and trailing edges. For example, in Wu's study of the Si/SiGe superlattice, the Ge composition change is gradual rather than sharp, as can be seen from Figure 1.14b. Clark *et al.* studied the junction abruptness in Au-catalyzed VLS Si/SiGe heterostructures and concluded that the width of the transition region is on the order of the nanowire diameter (*e.g.*, ~20 nm). This effect, termed the reservoir effect, can be explained by the finite time it takes to deplete the existing nanowire material from the liquid alloy, and re-establish the eutectic condition with the new material. During this transition period both types of materials forming the heterojunction will be incorporated into the grown nanowire, leading to a region with mixed composition ratios.[94] In Clark's experiment, Si nanowires were grown in an LPCVD chamber with a mixture of SiH_4 and H_2 gas, while GeH_4/H_2 was introduced during the growth and turned off some time later to produce a SiGe segment

within Si nanowires. With annular dark field scanning transmission microscopy (ADF STEM), it was found that the intensity profile of the Ge element can be fitted with an error function (leading) and exponential decay (trailing). Clark *et al.* observed that the characteristic length in both edges (Figure 1.16) scales with nanowire diameter in the range 10–40 nm. An intuitive explanation for this linear dependence is that the transition time is proportional to the number of atoms in the alloy (which scales with the alloy volume, d^3, where d is the diameter) divided by the liquid/solid interface area (which scales with d^2) that forms the growth front.

These observations suggest that in order to obtain a sharp axial nanowire heterostructure it is necessary to employ a catalyst with low solubility of the target semiconductor material. One approach in the context of VLS nanowire growth is the use of a metal catalyst with low solubility for the semiconductor material, such as In, Sn and Bi.[95] Another route is to modify the phase diagram *via* metal alloying. For example, adding Ga into Au has been demonstrated to improve the Si/Ge heterojunction abruptness through the reduction of Si(Ge) eutectic composition in the Ga/Au alloy.[96]

An alternative approach is to control the growth conditions so that the metal/semiconductor alloy stays in the solid form during the growth process but close to the eutectic point. Since solid solubility is generally much lower than liquid solubility for the same materials considered the reservoir effect can be greatly mitigated. For example, Wen *et al.* reported a transition width of only ~1.3 nm in a Si/Ge nanowire heterostructure with a diameter of 17 nm.[73] However, a drawback of the VSS growth mode is the significantly lower growth rate (typically 10 to 100 times slower[79]). To improve the growth rate, Al was added to the Au catalyst to raise the eutectic temperature so that a high growth temperature could be employed to obtain reasonable growth rate while still keep the alloy the solid form. Figure 1.17 shows a representative TEM image of the Si/Ge axial heterostructure nanowire with the Au catalyst still on the tip of the nanowire. Figure 1.18 is a collection of frames from recorded *in situ* TEM movies of the Si/Ge nanowire growth, from which clear facets on the alloy can be seen, indicating that the alloy stays in the solid phase. The transition width between Si and Ge segments of the nanowire was inferred from EDS line scan measurements, shown in Figure 1.17. It is also possible to adopt the VSS mode only for the transitional region while employing VLS for the rest of the part to maintain an overall high growth rate (Figure 1.18). Solidification of the catalyst alloy, as proved by the formation of facets, is clearly seen as the growth temperature drops from 570 to 503 °C, indicating the transition from the VLS mode to the VSS mode.

1.5 *In Situ* Doping of Nanowires

In integrated circuits, semiconductor nanowires can act as useful and versatile building blocks, particularly if different doping types are available with atomic level control. The geometry of the nanowires, *i.e.*, high aspect ratio, makes conventional doping methods such as diffusion and ion

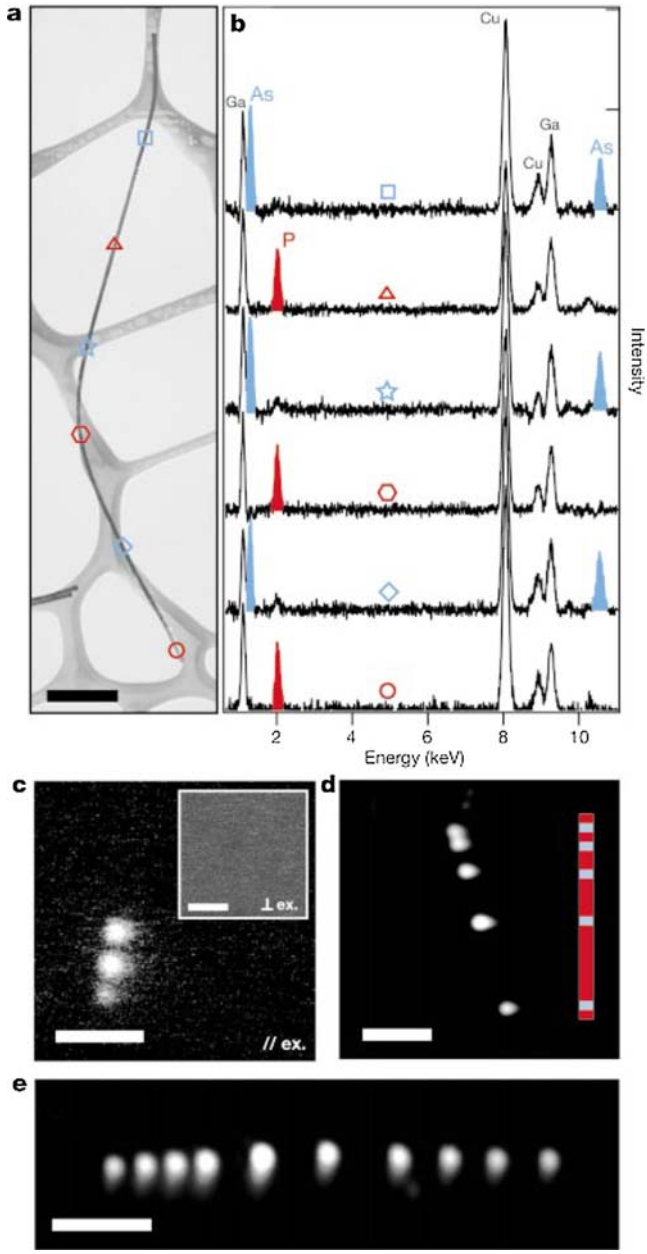

Figure 1.15 (a) TEM image of a ~20 nm-diameter $(GaP/GaAs)_3$ nanowire superlattice. Scale bar: 300 nm. (b) Elemental profile of the superlattice along the nanowire measured by EDS analysis, showing a distinct, periodic modulation of the nanowire composition along its entire length, with three uniform periods of GaP, separated by three uniform periods of GaAs. (c) Photoluminescence image of

implantation challenging. Instead, a more practical approach is through *in situ* doping of semiconductor nanowires during growth. The basic principle is simple and both n-type and p-type doping have been realized in commonly used semiconductor nanowires, including Si, Ge, SiC, III–V, II–VI compound and metal oxides.[97]

Similar to the different processes involved in semiconductor material (*e.g.*, Si) deposition during nanowire growth discussed earlier in Figure 1.8, dopant atoms can be incorporated into the nanowires at the same time *via* two modes, namely, radial deposition and axial incorporation through the eutectic alloy. Wallentin *et al.* proposed a theoretical model to analyze the different dopant incorporation processes, as illustrated in Figure 1.19. Specifically, the model examines several competing processes: the dopant flux from vapor to liquid, J^{LV}, the flux from liquid to solid, J^{LS}, and re-evaporation from liquid to the vapor, J^{EV}. The segregation of dopants at the liquid/solid interface also plays an important role in determining the rate at which dopants go into the nanowire. Based on the dopants solubility in the liquid alloy and the segregation coefficient C_S/C_L where C_S and C_L are, respectively, the dopant solubility in solid and in liquid, dopants can be divided into two main categories. Type A dopants have low solubility and high segregation coefficient such that the limiting process for the axial dopant incorporation will be the flux from vapor to liquid, J^{LV}. A direct implication is that by increasing the dopant precursor partial pressure, the doping level in the resulting nanowires can be enhanced. A typical example of such a case is P doping in Si nanowires using PH_3. To the contrary, type B dopants have high solubility and low segregation coefficient so the dopant concentration in the nanowire is mainly determined by the segregation coefficient and not the vapor precursor concentration. Examples of type B dopants include Sb doping in Au catalyzed Ge nanowires and Si doping in Ga seeded GaAs nanowires.[97]

It is also of great interest to study the radial distribution of the dopants in nanowires as the dopants (by definition impurities) may not be distributed uniformly at such nanoscales. *Ab initio* simulations have suggested that dopants have a tendency to segregate towards the surface to passivate the dangling bonds there, an effect termed as "self-purification".[98] The larger

a nanowire from the same sample as shown in (a and b). The three bright regions correspond to the three GaAs (direct bandgap) regions, while the dark segments are from the GaP (indirect bandgap) regions. Scale bar: 5 μm. (d) Photoluminescence image of a 40 nm-diameter multi-segment GaP/GaAs superlattice. Scale bar: 5 μm. (e) Photoluminescence image of a 21-layer superlattice, $(GaP/GaAs)_{10}GaP$, showing a group of four equally spaced spots on the left, two in the middle with larger gaps, and another set of four with equal spacing on the end. The superlattice is ~25 μm in length. Reproduced with permission from ref. 16. Copyright (2002) Nature Publishing Group.

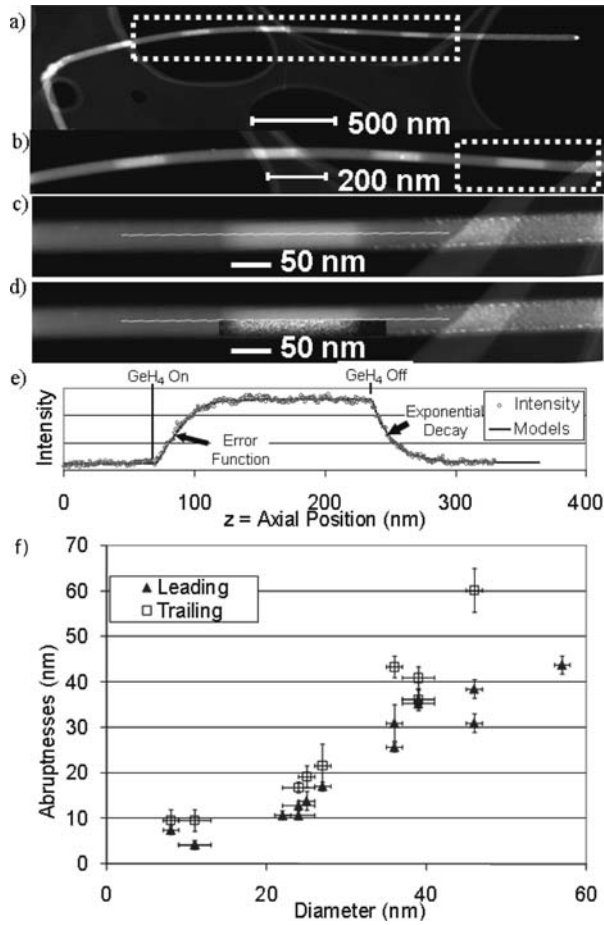

Figure 1.16 (a–c) Annular dark-field STEM images of a Si/Si$_{1-x}$Ge$_x$ hetero-nanowires consisting of 6 Si/Si$_{1-x}$Ge$_x$ blocks separated by Si segments at different resolutions revealing the non-abruptness of the Si/Si$_{1-x}$Ge$_x$ interface. (d) ADF-STEM image with overlay of Ge EDS map revealing that the HAADF image is dominated by atomic number contrast. (e) The intensity profile of the last Si/Si$_{1-x}$Ge$_x$ segment reveals asymmetric interfaces can be described by an error function (leading) and an exponential decay (trailing). (f) Abruptness of leading and trailing interfaces as a function of diameter for Si/Si$_{1-x}$Ge$_x$ nanowire heterostructures. Reproduced with permission from ref. 94. Copyright (2008) American Chemical Society.

segregation energy in unpassivated nanowires compared with surface passivated ones also confirms this trend.[98] Directly measuring the radial doping profile inside the nanowires is no doubt challenging due to the size of the of the sample, but recent advances have provided clear evidence of the non-uniform nature of dopant distribution inside the nanowires. In one

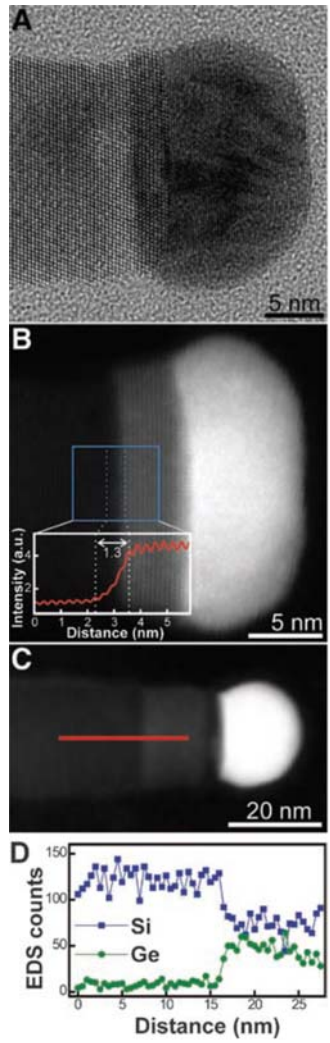

Figure 1.17 (A) High-resolution TEM image of a Si–Ge heterojunction nanowire. A Si wire (length 500 nm, diameter 18 nm) was grown rapidly using VLS at 510 °C with 1×10^{-5} Torr Si_2H_6 for 2 h, then cooled and grown for several minutes in the VSS mode at 360 °C, followed by growth of a Ge segment at 360 °C with 5×10^{-6} Torr Ge_2H_6 for 16 min. (B) HAADF-STEM image of a wire (diameter 17 nm) grown under the same conditions. Inset: the intensity profile across the interface, averaged over a 5 nm strip along the midpoint of the wire. The width of the interface is 1.3 nm. (C) HAADF-STEM image of a $Si/Si_{1-x}Ge_x$ nanowire (diameter 21 nm). Si was grown at 510 °C and 1×10^{-5} Torr Si_2H_6 for 2 h; $Si_{1-x}Ge_x$ was grown at 430 °C with 2×10^{-6} Torr Si_2H_6 and 1×10^{-7} Torr 20% Ge_2H_6; then Si was grown at 510 °C and 2×10^{-6} Torr Si_2H_6. (D) EDS line profile of Si and Ge through the $Si/Si_{1-x}Ge_x$ junction, as indicated in (C), showing a sharp transition (less than 2 nm) from Si to SiGe. Reproduced with permission from ref. 73. Copyright (2009) American Association for the Advance of Science.

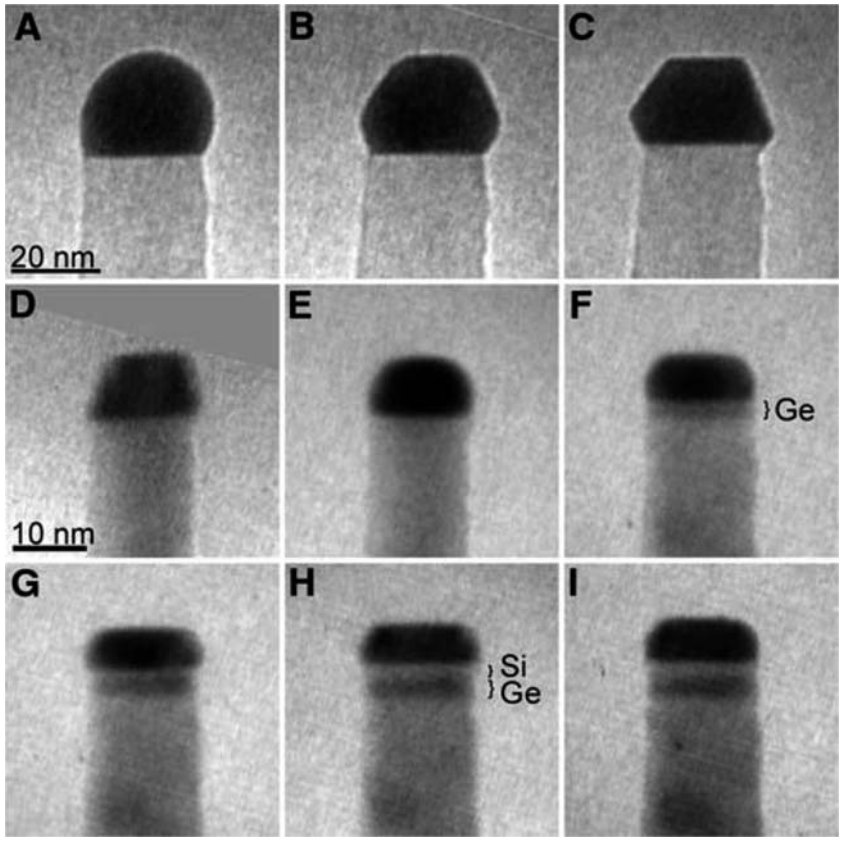

Figure 1.18 (A–C) Frames extracted from a movie recorded during growth of a Si nanowire (diameter 28 nm) in 3×10^{-5} Torr disilane as the temperature was reduced from 570 to 503 °C: (A) immediately before solidification of the catalyst (507 °C); (B) just after solidification (503 °C), which is evident from the faceted shape of the catalyst; (C) 14 s after (B). (D–I) Formation of a Si–Ge–Si heterojunction in a Si nanowire (diameter 14 nm). The Si nanowire in (D) was first grown at 510 °C with 1×10^{-5} Torr Si_2H_6 for 2 h and then cooled to 360 °C. The faceted surface after cooling indicates the solid state of the catalyst. (E) After flowing 5×10^{-6} Torr Ge_2H_6 at 360 °C for 1 min, Ge growth has begun and the catalyst has become less sharply faceted. (F) After 7 min, formation of a thin Ge layer that appears as a dark band at the Si–catalyst interface. (G) After 8.5 min of Si growth at 360 °C and 1×10^{-5} Torr Si_2H_6. (H) After 14 min of Si growth, the catalyst has resumed the strong facets on its surface seen in (D). (I) The catalyst was exposed to 5×10^{-6} Torr Ge_2H_6 at 360 °C for 1 min again, resuming the shape seen in (F). Reproduced with permission from ref. 73. Copyright (2009) American Association for the Advance of Science.

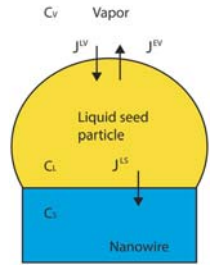

Figure 1.19 Schematic of the different fluxes during vapor–liquid–solid nanowire growth. Reproduced with permission from ref. 97. Copyright (2011) Cambridge University Press.

study performed by Garnett *et al.*, the gate capacitance of a boron-doped Si nanowire transistor was directly measured and the radial dopant profile was extracted from high frequency capacitance–voltage measurements.[99] The authors observed an apparent non-uniform dopant distribution profile with much higher impurity concentration at the surface, consistent with the self-purification hypothesis.[99] In an independent study carried out roughly at the same time, Xie *et al.* performed a series of experiments on doped Si and Ge nanowire transistors to probe the dopants location.[100] In this study, Si and Ge nanowires were heavily doped during growth with PH_3 or B_2H_6 gas and then fabricated into planar field effect transistors. The nanowire diameter was then reduced by low temperature oxidation and subsequent oxide removal. One such cycle resulted in a ~3 nm decrease in nanowire diameter. The effective doping concentration of the nanowire was then calculated through the threshold voltage of the transistors. Figure 1.20 shows results from these experiments. Heavily doped nanowires will have a high threshold voltage, $|V_{th}| > 10$ V, while lightly doped ones will have reduced V_{th}. Thus nanowires with dopants accumulated near the surface will behave differently from the ones with uniformly distributed dopants. It was found that above a critical diameter, ~23 nm, the oxidation/etching cycle did not alter the threshold voltage of the transistors while nanowires of smaller sizes exhibited a large shift in threshold after diameter reduction, with a reduced effective doping concentration. These results suggest that, for the larger nanowires, the dopants are incorporated uniformly in the nanowire similar to bulk material growth, while for smaller nanowires the dopants are more concentrated in the surface area. Additionally, nanowires with initial diameters above the critical dimension did not exhibit threshold shifts even after their diameters had been reduced to below the critical dimension through multiple diameter reduction cycles, verifying that the non-uniform doping effect originated during growth, which is consistent with the *C–V* measurement results reported in Garnett *et al.*'s work.[99]

Similar to catalyst atom detection in a nanowire, atom probe tomography was also used to analyze the location and concentration of dopants. In a study by Perea *et al.* on Ge nanowires with *in situ* PH_3 doping, the

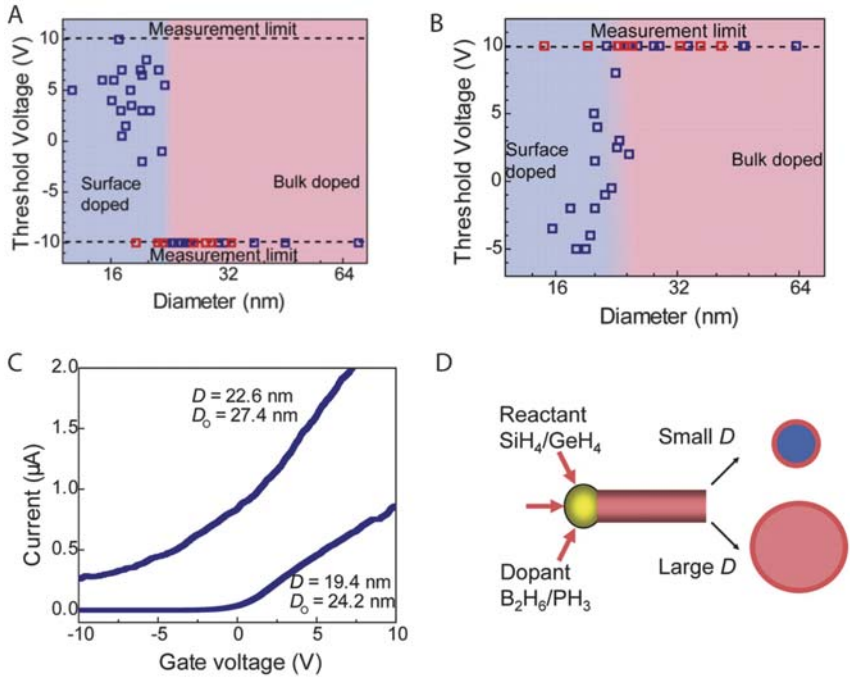

Figure 1.20 (A and B) Diameter dependence of the threshold voltage for P-doped (A) and B-doped (B) nanowires, indicating different effective doping levels under otherwise identical growth conditions. Blue (red) squares represent data from NWs after oxidation and etching (control nanowires). (C) Comparison of *I–Vg* curves at V_{sd} = 1 V between P-doped Si NWs with different diameters after 4 cycles of oxidation and etching. *D* (D_0) is the diameter after (before) oxidation and etching. (D) Schematic of dopant distribution. Pink and dark pink shaded parts together represent heavily doped regions (darker = higher), and blue corresponds to a lightly-doped or intrinsic region. Reproduced with permission from ref. 100.

reconstructed tomographic image revealed a heavily doped shell and lightly doped Ge core[54] (Figure 1.21). Owing to the presence of sidewall deposition under the Ge nanowire growth condition, an axial doping gradient was also observed by Perea *et al.*, although this effect is mainly caused by the tapered geometry due to the non-uniform shell thickness. In Perea *et al.*'s study with substantial shell deposition, the non-uniform doping profile could be explained by the different dopant incorporation mechanisms as discussed in Wallentin *et al.*'s model.[97] Specifically, the doping concentration is determined by the relative dissociative chemisorption rate of PH_3 and GeH_4. The PH_3 decomposes at a faster rate than GeH_4 at vapor/solid interface, leading to the formation of a heavily doped shell. On the other hand, core doping is realized *via* VLS process in which GeH_4 decomposition at the vapor/liquid interface is catalyst mediated, resulting in a relatively lightly doped core.

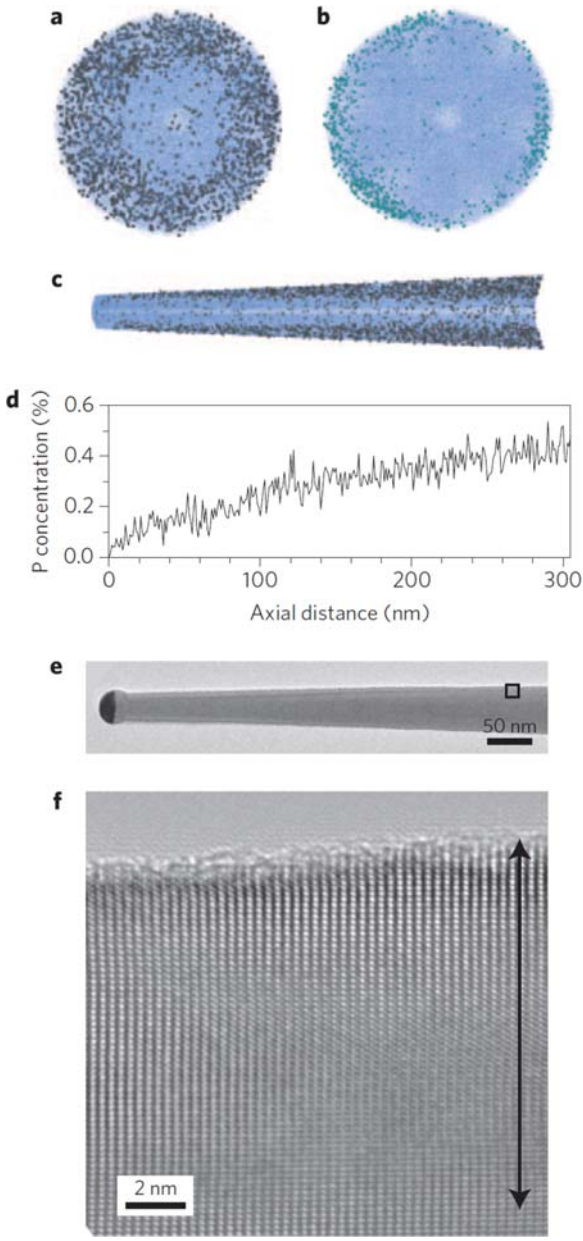

Figure 1.21 (a and b) End-on view of a Ge nanowire (43 nm in diameter) showing the distribution of phosphorus (a, grey spheres) and oxygen (b, light blue spheres) in germanium (blue dots). (c) Side view of nanowire cross-section (2 nm thick). (d) Average phosphorus concentration along the growth axis. (e) Bright-field TEM image of a phosphorus-doped germanium nanowire. Scale bar: 50 nm. (f) High-resolution bright-field TEM image of a phosphorus-doped shell region inside the box in (e). The large black arrow (12 nm) illustrates the extent of the phosphorus-doped shell. Scale bar: 2 nm. Reproduced with permission from ref. 54. Copyright (2009) Nature Publishing Group.

Another important effect in doped nanowires due to the small sample size is the increased activation energy for dopant ionization. This effect can be explained in terms of the reduction of the effective dielectric constant compared to that of the bulk material. In a study by Bjork *et al.*, phosphorous-doped n-type Si nanowires with different doping concentrations and different diameters were prepared and carefully analyzed, by controlled introduction of PH_3 during synthesis and analyzing the resistivity of the nanowires.[101] Surprisingly, a negative correlation was found between the nanowire diameter and its resistivity, even though the nominal doping conditions during growth are the same for all nanowires. After taking into account other factors such as the surface depletion effect, the nanowire resistivity and the nanowire electric diameter (the physical diameter subtracted by the surface depletion width) can be fitted into a universal curve for all nanowires with different doping concentrations and different diameters (Figure 1.22). Assuming constant carrier mobility in these nanowires, the results suggest a reduced free carrier density with decreasing nanowire sizes. This phenomena was in turn explained by a model developed by Diarra *et al.*[102] In this model, the ionization energy of the dopant atoms in nanowires was found to be increased due to less Coulomb screening from the surrounding media (*e.g.*, air) with a low dielectric constant, an effect termed as dielectric confinement. The increase of the dopant activation energy can be expressed in the following form:

$$E_I - E_I^0 \approx \frac{2e^2}{\varepsilon_{in} R} \frac{\varepsilon_{in} - \varepsilon_{out}}{\varepsilon_{in} + \varepsilon_{out}} F\left(\frac{\varepsilon_{in}}{\varepsilon_{out}}\right) \propto \frac{1}{R} \tag{1.2}$$

where E_I and E_I^0 are dopant activation energy before and after considering the dielectric confinement, respectively, ε_{in} and ε_{out} are dielectric constants of the semiconductor and the surrounding material, e is the elemental charge, and R is the nanowire radius. It can be readily seen that dopants in these nanostructures will experience an increased activation energy compared to dopants in bulk materials, with the increase in activation energy inversely proportional to the nanowire size. The observation of increased dopant activation energy in such nanostructures is significant as many applications require heavily doped regions for reasons ranging from forming effective Ohmic contacts to creating strong electrical fields. On the other hand, since the dielectric confinement effect that leads to increase in activation energy is caused by the low-k (*e.g.*, air) medium surrounding the nanowire, this problem can be effectively mitigated by surrounding the nanowire with another medium instead of air, such as a high-k material.

It is also possible to switch dopant precursors during nanowire growth in a similar fashion as that used during nanowire heterostructure formation. For example, by pulsing the flow rate of PH_3 during Si nanowire growth, Yang *et al.* realized alternating n and n+ doped segments in the same nanowire. Figure 1.23 shows the resulting Si nanowires with different number of n+ segments and lengths. Scanning gate microscopy (SGM) was employed to

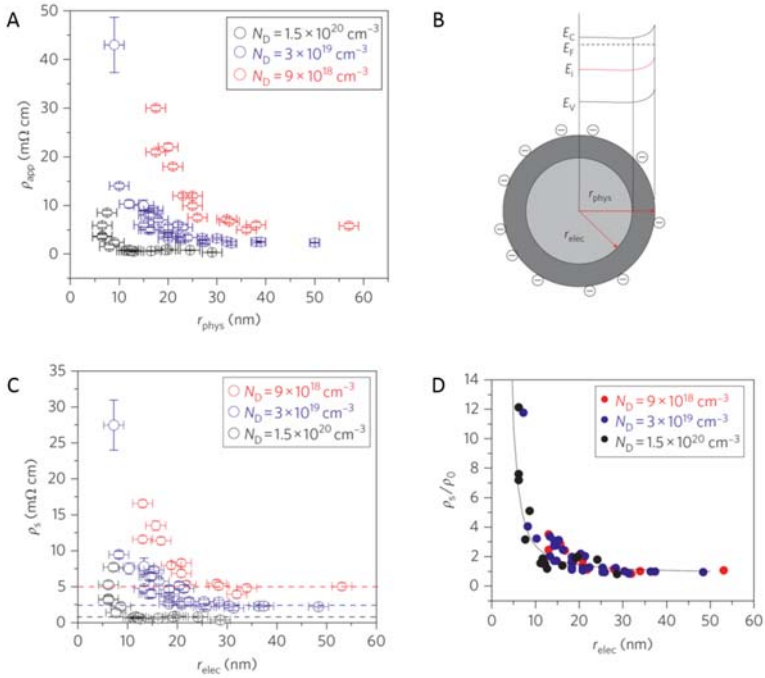

Figure 1.22 (A) Band diagram and schematic illustration showing how the interface states of density D_{it} attract negative charge from the n-type silicon nanowire and cause a depletion zone at the surface. (B) Electrical radius as a function of physical radius. (C) Nanowire resistivity as a function of electrical radius. The measured resistivity data were corrected for the surface depletion effect using an interface trap density of 6×10^{12} cm^{-2} eV^{-1}. The resistivity increases drastically as the electronic radius is decreased. (D) Normalized resistivity as a function of the electronic radius at different doping levels. The solid line is based on eqn (1.2). Reproduced with permission from ref. 101. Copyright (2009) Nature Publishing Group.

highlight the location of the n+ segments (which showed no gate response and appear as brighter regions).[2] Similar results were obtained by Schmid *et al.* by switching on/off PH_3 during Si nanowire growth to achieve alternating i/n segments.[103] Figure 1.24 shows SEM images of nanowires with different axial doping profile and segment lengths. The doped part can be identified by their brighter contrast under SEM. Similar techniques have been used to produce PIN structures in Si nanowires in both axial[27] and radial[104] configurations. Notably, the discussions on nanowire heterojunction abruptness and the reservoir effect also apply when studying the properties of junctions formed by heterogeneous doping, that is, the transitional width of different doping segments is finite and in general proportional to the nanowire diameter. This effect can be significant in nanowire

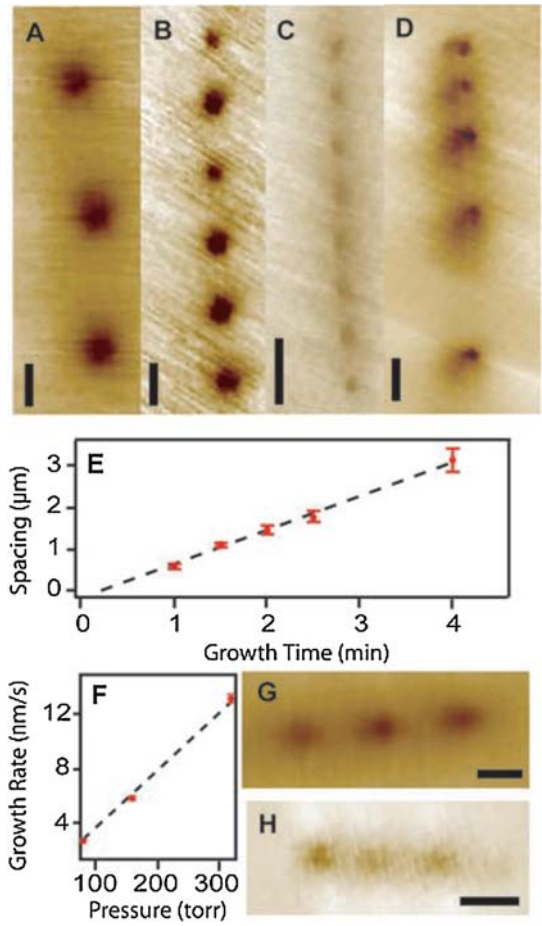

Figure 1.23 Scalable synthesis of modulation-doped nanowires. SGM images of n^+-$(n^-n^+)_N$ nanowires for (A) $N = 3$, (B) $N = 6$, and (C) $N = 8$, with growth times for the n/n+ regions of 1/3, 1/1, and 0.5/0.5 min, respectively. (D) SGM image of $N = 5$ nanowire, where the growth time for the n regions is 0.5 min, and n+ sections are 0.5, 1, 2, and 4 min. Scale bars, 1 μm. (E) Repeat spacing *versus* growth time at total pressure of 320 Torr. (F) Growth rate *versus* growth pressure. SGM images of n^+-$(n^-n^+)_3$ modulation-doped nanowires synthesized with total pressures of (G) 160 and (H) 80 Torr. The growth time for each n and n+ region is 15 s. Scale bars: 100 nm. Reproduced with permission from ref. 2. Copyright (2005) American Association for the Advance of Science.

applications since in emerging electronic devices, such as tunneling transistors, the on-state current critically depends on the electrical field at the junction, which is in turn affected by abruptness of the doping profile. Simulation for a Ge based tunnel diode suggested that with a gradient of 1 nm per decade a tunnel transistor can still maintain 50% of its on-state current compared to the case with an ideally abrupt junction while 4 nm per

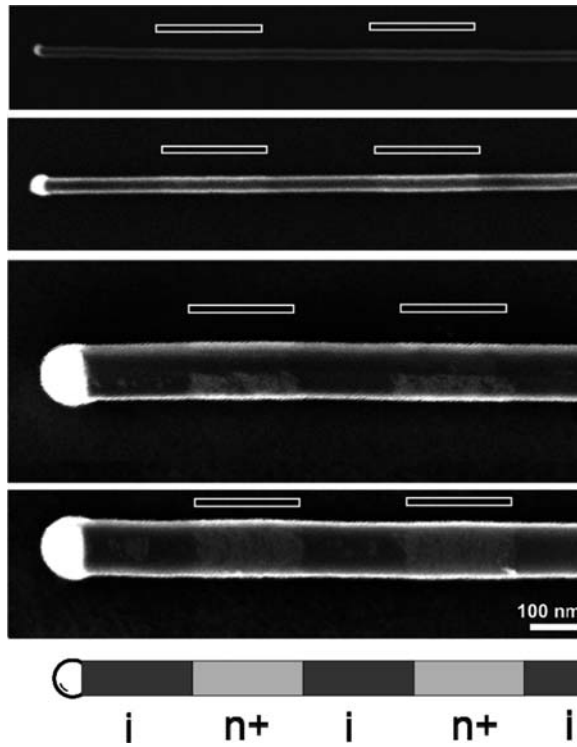

Figure 1.24 SEM images of SiNWs containing doped segments. The wires were grown at 440 °C at a SiH_4 partial pressure of 200 mTorr. The segments were doped by co-flowing 1 part PH_3 in 66 parts of SiH_4 for 60 s. The radii are (top to bottom) 11, 16, 55, and 55 nm. The scale bar is 100 nm. Areas of extended bright contrast correspond to the doped segments, as is indicated in the schematic at the very bottom. The locations of the doped segments are additionally indicated by bars. Reproduced with permission from ref. 103. Copyright (2008) American Chemical Society.

decade leads to an almost 10× reduction.[105] To reduce the transition width, efforts need to be paid to reduce the specific dopant's concentration in the liquid alloy analogous to the approaches taken to improve the junction abruptness in nanowire heterojunctions.

An interesting application of heterogeneous doping was demonstrated recently by Christesen *et al.* by combining doping modulation and selective etching.[106] Figure 1.25 shows the complex nanowire morphologies that can be obtained after KOH etching. The technique relies on the observation that the etching rate of Si by KOH is dependent on the doping level of the nanowire segment, so by creating regions with different doping levels along the nanowire a patterned morphology can be obtained simultaneously after a simple global wet etching step. The shapes of the transition regions can

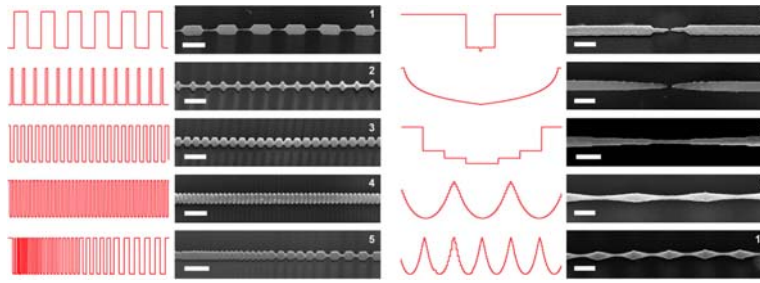

Figure 1.25 SEM images and phosphine flow profiles for the creation of Si nanowires with different morphology after a simple global wet etch. The measured phosphine flow profile used to encode the morphology of each segment is depicted in red to the left of each SEM image; all scale bars: 200 nm. The flow rates vary from 0 to 20 sccm for each NW. Reproduced with permission from ref. 106. Copyright (2013) American Chemical Society.

also be controlled by carefully designing the doping profile between nanowire segments. The spatial resolution of this technique is ~10 nm, which is likely determined by the minimal PH_3 pulse width and the reservoir effect, but can likely be improved through optimization of the growth parameters.

The addition of doping species can also affect nanowire growth depending on the material added and the process conditions. Among them, tapered nanowires due to unintentional thin film deposition on nanowire sidewalls are most commonly reported. Such reaction can be minimized by proper tuning of the growth conditions, but enhanced side wall deposition is often observed, especially in the presence of B_2H_6.[107] This is likely due to catalyzed decomposition of the semiconductor precursor with B_2H_6, an effect well known in the deposition of Si thin films.[108] A similar finding reported by Tutuc *et al.* was that a conformal P-rich shell can be present for Ge nanowires grown with PH_3.[109] In contrast, *in situ* Si nanowire doping by PH_3 and B_2H_6 with minimal disturbance to the growth rate and morphology has also been reported with optimized growth conditions.[100,103] An alternative route to achieve doping without incurring the tapered shape is to dope the nanowire surface without the semiconductor precursor, eliminating the thin film deposition altogether. For example, Greytak *et al.* successfully doped Ge nanowires after pure Ge nanowire elongation, with either PH_3 or B_2H_6 in the absence of GeH_4 to produce a self-limited layer of electrically activated dopant atoms.[75]

In addition to enhanced sidewall deposition, faceting can occur when dopants are present, depending on the growth conditions. Li *et al.* observed periodic sawtooth faceting on VLS grown Si nanowires when B_2H_6 is added to the precursor while intrinsic or n-type doped nanowires with PH_3 showed smooth surfaces instead. As shown in Figure 1.26, groups of {111} and {100} facets have been generated for Si nanowires grown with B_2H_6.[110] Subsequent growth experiments revealed that facets can form on existing smooth

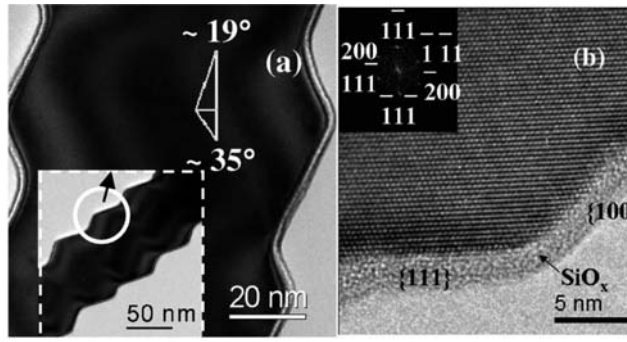

Figure 1.26 (a) HRTEM image of the sidewall facets in the B-doped region of an axial heterostructured p–n–i Si nanowire, viewed from the ⟨110⟩ direction; inset: image taken at low magnification and facet angles are indicated. (b) HRTEM image of the facet; inset: Fourier transform of the image. Reproduced with permission from ref. 110. Copyright (2009) AIP Publishing.

nanowires when B_2H_6 was on, suggesting that faceting occurred during the radial overcoating due to enhanced deposition at the vapor/solid interface. Overall these results indicate that *in situ* doping in nanowire growth is a complex subject and the addition of the dopants may affect the delicate growth chemistry and the morphology of the nanowires. As a result, the actual doping profile and the nanowire properties can be strongly affected by the seemingly innocent act of adding even small amounts of dopants, and it pays to have a clear understanding of the nanowire growth dynamics.

1.6 Beyond Individual Nanowire Growth

The synthesis of semiconductor nanowires has undergone tremendous development since the initial demonstrations. Many aspects of the nanowire growth can now be tailored to meet specific demands for a wide range of applications. In addition to the ability to tune the intrinsic nanowire properties such as material composition, morphology and doping profile, research has been carried out to develop more complex nanowire systems that include networks bridged by individual nanowires or circuits with integrated nanowire active components and electrodes by carrying out the nanowire growth dynamics in a controlled fashion.

1.6.1 Growth Site Control

A potential challenge of creating nanowires grown by the bottom-up VLS approach compared to using the top-down nanofabrication method is the former's lack of ability to control the positions of the nanowires precisely. A typical growth results in randomly distributed nanowire locations due to the

random distribution of the starting nanoparticles. To ensure position control, several efforts have been made to fabricate sub-10 nm nanowires using the top-down nanofabrication methods[111,112] although the diameter control and the quality of the nanowires are still not optimal. Since the ability to control the growth sites of nanowires is essential for heterogeneous device integration, it has become a key requirement for VLS nanowires if they are to be employed on a large scale in the semiconductor industry.

Since the nanowire growth is mediated by the metal nanoparticles in the VLS process, it is natural to try to control the nanowire growth sites by controlling the original catalyst nanoparticle positions. Sato *et al.* proposed to use a SiO_2 film as patterning mask for defining the Au catalyst position in the growth of GaAs nanowhisker as early as 1995.[113] The concept of patterned growth, or selective area growth, has been adopted by many groups in recent years and the results reported are promising with the use of Au nanoparticle and advanced lithography techniques such as e-beam lithography. Figure 1.27(a) shows a high density array of vertical VLS grown InP nanowires.[114] The nanowires were catalyzed by Au nanodots with a 45 nm diameter and patterned using e-beam lithography. Similar results were obtained for InAs nanowire arrays.[47] Importantly, for catalyzed nanowire growth, there are many possible approaches to define the location of the metal particles. For example, Figure 1.27(b) and (c) shows a microcontact printing method developed by Hochbaum *et al.* to transfer a poly-L-lysine film onto selected regions on a Si substrate.[70] Poly-L-lysine was used to attract the Au seeds so only the patterned regions were dispersed with Ag nanoparticles to realize patterned Si nanowire growth. Some other approaches involve the use of nano-manipulation techniques by atomic force microscopy,[115] metal deposition through alumina templates[116] and nanosphere lithography (NSL),[117] just to name a few. Notably, even for non-VLS based, catalyst-free nanowire

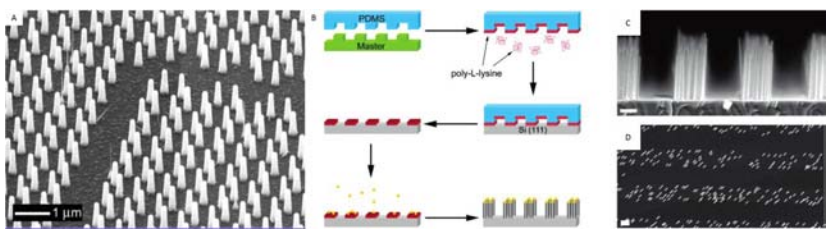

Figure 1.27 (A) SEM micrograph of a nanowire array where EBL and metal lift-off have been used define the pattern of growth-catalyzing gold particles. This SEM image was made using a 45° viewing angle. Reproduced with permission from ref. 114. Copyright (2004) American Chemical Society. (B) Schematic of PDMS (Polydimethylsiloxane) patterning of Au colloids. (C) Cross-sectional SEM image of PDMS patterned Si nanowire growth, and (D) plane-view SEM image of the same. Scale bars: 1 μm. Reproduced with permission from ref. 70. Copyright (2005) American Chemical Society.

growth processes, the concept of patterning may still be valid and patterned growth has been demonstrated with the use of masking materials such as a patterned SiO_2 film.[58]

1.6.2 Branched Nanowires

Branched or tree-shaped nanowires can be obtained by dispersion of catalyst particles on the first grown nanowires (trunk) and re-introduction of the growth precursors for a second growth stage. Figure 1.28 shows the first demonstration of branched Si nanowires, by Wang *et al.*[118] In this experiment, the backbone Si nanowires were first synthesized with the ⟨111⟩ growth orientation followed by the deposition of Au nanoparticles on the nanowire backbone and a second growth using the same process. A TEM study on the trunk and branch positions revealed that they both followed the equivalent ⟨111⟩ orientations, thus proving epitaxial nature of the branch growth. It is possible to create more complex structures with multiple stages of branch growth following the same principle, such as the two-stage branched nanowires shown in Figure 1.28(e). Branched nanowires were also demonstrated with other materials, such as GaN[118] and GaP.[119] These branched epitaxial nanowire structures could in turn be used for novel electronic and optoelectronic devices such as p–n diodes constructed by oppositely doped backbone and branches.

1.6.3 Kinked Nanowires

The concept of designing the morphology and function of nanowire structures can be further extended to the construction of intentionally kinked nanowires. Tian *et al.* demonstrated the synthesis of secondary building units (SBUs) consisting of two straight single-crystalline arms connected by one fixed 120° joint in Si nanowires (Figure 1.29).[120] These kinks are created by introducing a perturbation during the normal Si nanowire growth. One type of perturbation includes purging and re-introducing the semiconductor reactants (SiH_4 in this case). It was found that if the purge time is sufficiently long (*e.g.*, 15 s) then the Si concentration in the eutectic alloy will drop to a level low enough for the nanowire elongation to stop. Resuming the supply of the reactant will initiate supersaturation again and re-start the nanowire growth process, but the nucleation may occur at another equivalent ⟨112⟩ direction instead thus forming a kink with the existing Si segments. Reduction of the purge time decreases the yield of kinks, especially for nanowires with larger diameters, possibly because the concentration in the alloy is high enough to sustain continued elongation. However, the perturbation does leave behind a node in the nanowire, which is defined as the segment with increased nanowire diameter, as a result of flattening of the catalyst droplet (Figure 1.29e and f). Tian *et al.* also demonstrated the ability to combine this technique with *in situ* doping modulation. With PH_3 or B_2H_6 added in the growth of the

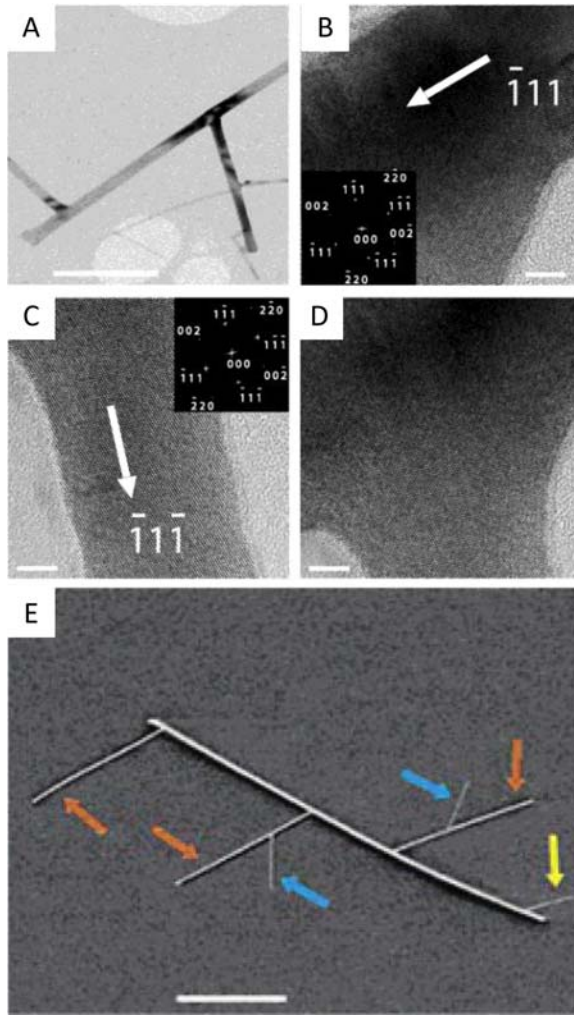

Figure 1.28 (A) TEM image of a branched NW structure with two branches (scale bar: 250 nm), and lattice-resolved TEM images of the (B) backbone, (C) branch, and (D) junction. Scale bars: 5 nm. (E) SEM image of a hyperbranched SiNW structure. The first-generation and second-generation branches are indicated by orange and blue arrows, respectively. The yellow arrow indicates a 10 nm Si nanowire (from second-generation growth) grown from the backbone. Scale bar: 1 μm. Reproduced with permission from ref. 118. Copyright (2004) American Chemical Society.

different nanowire segments, a kinked nanowire PN junction can be obtained. A similar strategy can be readily used to achieve different doping concentrations within one-kinked nanowires to form transistors. Since kinked nanowires can be grown to have an acute angle between segments, which resembles probes in shape, nanowire sensors were a natural application. Demonstration of biological and chemical sensing ability has been realized with simple pn-junction[43] or transistor configurations[38,39] (Figure 1.30). Owing to its nanoscale dimension, intracellular sensing and signal recording can be achieved with minimal disturbance to the biological cell structure. It is also worth noting that this morphology controlling technique is also applicable to other materials, such as Ge or CdS nanowires.[120]

1.6.4 Connecting the Nanowires Together

Finally, an interesting research direction is to not only fabricate individual devices with VLS grown nanowires but also to use the nanowires to form interconnects so that, potentially, whole circuits can be fabricated in a bottom-up fashion. This idea is enabled by exploiting directional epitaxy during the growth of nanowires so that not only the direction but also the electrical integrity of the grown nanowires with the "substrate" can be controlled. One example of this approach is to grow nanowires from a sidewall to form bridges between a pair of electrodes. For example, starting with a (110) Si SOI substrate, He *et al.* performed a vertical etch to create (111) sidewalls as the growth sites and demonstrated epitaxial Si nanowire bridges[121] (Figure 1.31). The vertical growth confirmed that the Si nanowires indeed followed the ⟨111⟩ growth direction from the sidewall and the growth can be extended across the gap to the opposite side. Subsequent TEM analysis further revealed that these Si nanowires would grow backwards after making a solid contact at the opposite side, but still maintaining the ⟨111⟩ orientation with Au at the tip (Figure 1.31c).

Another interesting experiment attempted to make interconnects with nanowires growing from two adjacent sides, which requires accurate control of the growth sites for the nanowires to reach each other. In a study by Dalacu *et al.* using InAs nanowires epitaxially grown on InP substrates,[122] a two-step selective area epitaxial process using SiO_2 as the masking layer was employed. Starting from the (001) InP substrate, the first epitaxial step deposits lines of InP ridges with (111) sidewalls. Then the catalyst metal particles, Au in this case, were patterned and deposited on the sidewall of the InP ridges through an evaporation and liftoff process. The locations of the metal catalysts determine the nanowire growth sites while the (111) surface promotes epitaxial, vertical growth with respect to the sidewall. Carefully patterned Au particles were deposited on both sides of the ridge, so two

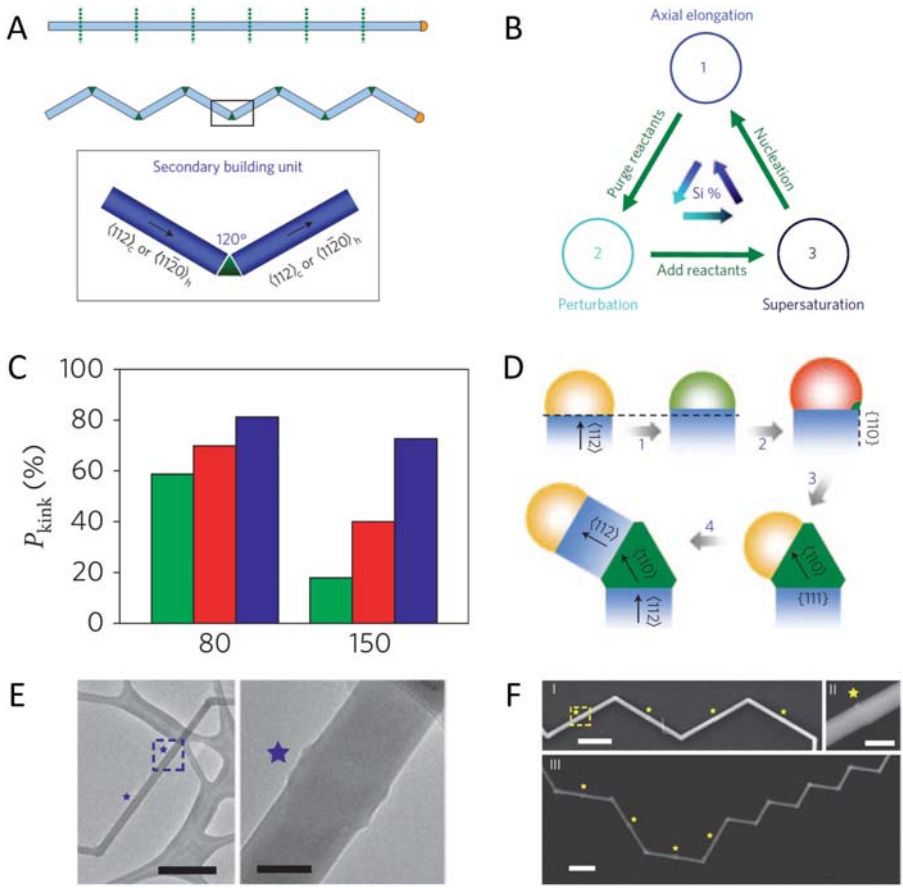

Figure 1.29 (A) Schematic of a coherently kinked nanowire and the secondary building unit (SBU), which contains two arms (blue) and one joint (green). (B) Introduction of a SBU by stepwise synthesis. The color gradient accompanying the innermost blue arrows indicates the change of silicon concentration during synthesis of a kinked silicon nanowire. (C) Kink frequency (P_{kink}) histogram for 80 and 150 nm diameter silicon nanowires grown with different purge durations. Green, red and blue bars denote results from 1, 3, and 15 s purges, respectively. (D) Schematic illustrating the key stages of kink formation. Arrows 1–4 denote purge, re-introduction of reactant, joint growth and subsequent arm growth, respectively. (E) TEM images at low (left panel) and high (right panel) magnification of one 80 nm-diameter silicon nanowire segment subjected to a 1 s purge. The blue stars mark incipient kinks or nodes, and the dashed square corresponds to the region where the right panel was recorded. Scale bars, 500 (left) and 50 nm (right). (F) SEM images of silicon nanowires with modulated kinks and incipient kinks (starred nodes). I: a designed $(\text{kink-node})_m$ structure; II: enlargement of one node from the region indicated by the dashed yellow square in I; III: a $(\text{kink-node})_m(\text{kink})_n$ structure, where m and n are integers. Scale bars in I, II and III: 1, 0.2 and 1 μm, respectively. Reproduced with permission from ref. 120.

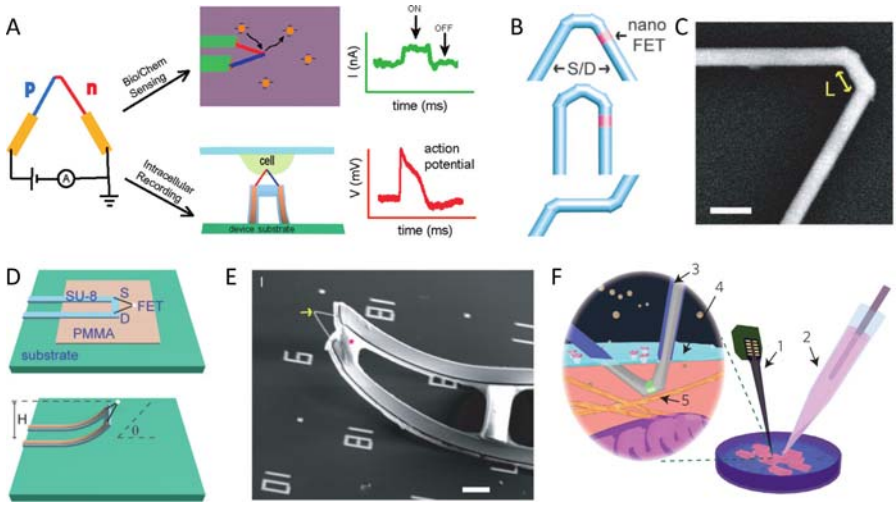

Figure 1.30 (A) Schematic of a kinked nanowire probe with an integrated pn diode and its sensing applications. Reproduced with permission from ref. 43. Copyright (2004) American Chemical Society. (B) Schematics of 60° (top) and 0° (middle) multiply kinked nanowires and *cis* (top) and *trans* (bottom) configurations in nanowire structures. The blue and pink regions designate the source/drain (*S*/*D*) and nanoscale FET (field effect transistor), respectively. (C) SEM image of a doubly kinked nanowire with a *cis* configuration. *L* is the length of segment between two adjacent kinks. Reproduced with permission from ref. 38. Copyright (2010) American Association for the Advance of Science. (D) Schematics of a 3D, flexible nanowire probe fabrication. Patterned poly(methyl methacrylate) (PMMA) and SU-8 microribbons serve as a sacrificial layer and flexible device support, respectively. The dimensions of the lightly doped n-type silicon segment (white dots) are ~80 by 80 by 200 nm^3. *H* and θ are the tip height and orientation, respectively. (E) SEM image of an as-made device. (F) Schematic illustrating the general experiment set-up with a free-standing nanowire probe as an intercellular recording device. The probe (1) with an integrated kinked nanoFET is mounted on an XYZ micromanipulator to target selected cells and record IC signals; a patch-clamp pipette (2), which is also mounted on a manipulator, can be used to monitor the same cell simultaneously. The nanowire is coated with a phospholipid layer (3) to facilitate penetration through the cell membrane (4) so that the nanoFET (5) is inside the cytoplasm. Reproduced with permission from ref. 39.

nanowires growing from each side of the ridge can merge with each other when the nanowire growth length is sufficient. In an ideal situation, when the sizes of the catalyst particles match perfectly, the two nanowires should merge tip-to-tip since the nanowire growth rate was found to have a negative correlation with the diameter of the starting catalyst particle.[123] Indeed, tip-to-tip merge was verified (Figure 1.32b–f) in some cases. SEM studies

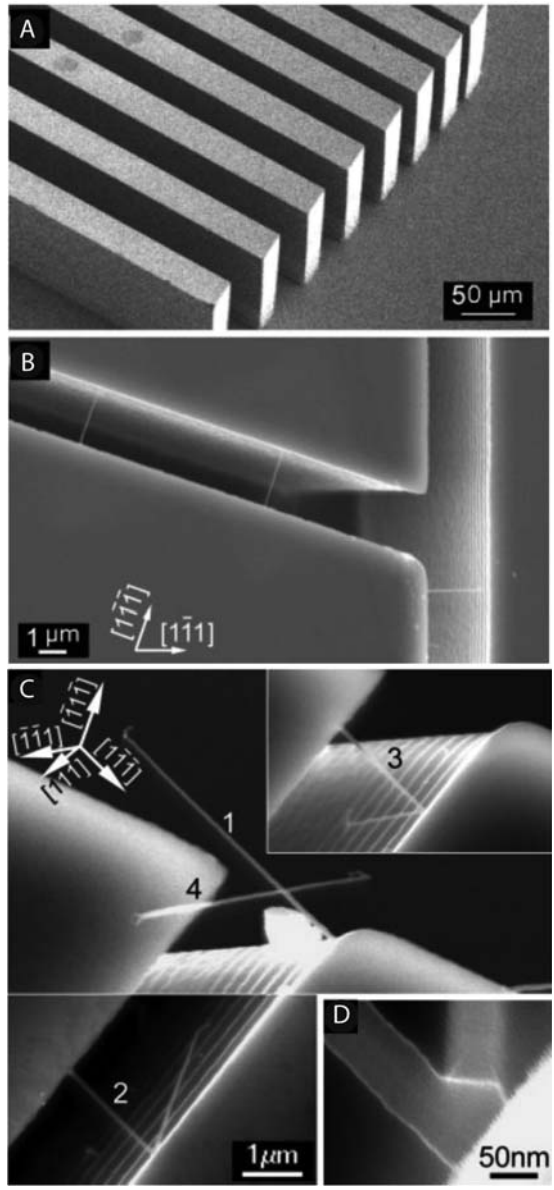

Figure 1.31 (A) SEM image of a group of parallel trenches formed on a (110) SOI (silicon on insulator) wafer. (B) SEM image of nanowire bridges formed in the micro-trenches. (C) SEM images showing connections between the Si nanowires and the trench sidewalls. (D) A magnified view of the wire–sidewall interface. Reproduced with permission from ref. 121. Copyright (2005) Wiley-VCH Verlag GmbH.

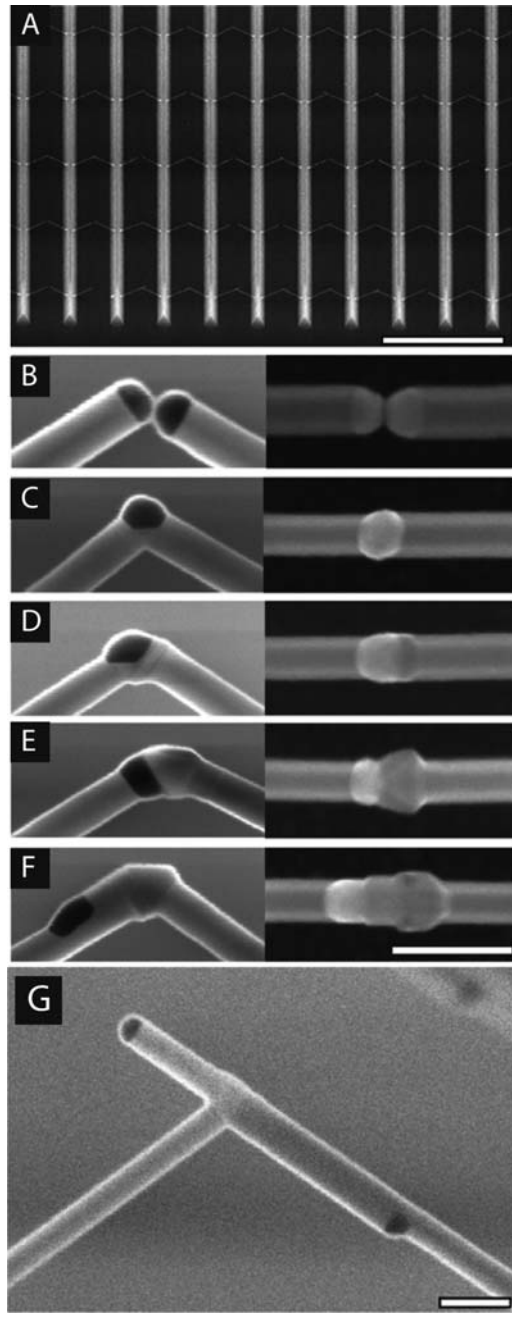

Figure 1.32 (A) SEM image viewed at 45° showing 100 InAs nanowire pairs grown on an array of InP ridges pitched at 4 μm. Scale bar: 10 μm. (B–F) SEM images viewed in cross-section (left panel) and plan view (right panel) of the different stages during growth of intersecting nanowires, highlighting the different configurations of the Au catalyst. (G) Closed-up SEM image showing a pair of connected nanowires. Scale bar: 100 nm. Reproduced with permission from ref. 122.

further revealed that after merging the InAs nanowires will grow back along one of the nanowires (Figure 1.32f). This can be explained by the fact that the two eutectic alloys effectively become one and it becomes more energetically favorable to continue the nanowire growth following an existing liquid/solid surface. On the other hand, if one nanowire grows faster than the other in the pair, the nanowires will merge tip to sidewall. In this case, the longer nanowire will continue to grow along its original direction since its growth was never disturbed, while the shorter nanowire, after having its eutectic merged with the surface of the longer one, will continue its growth along the longer nanowire by utilizing the existing liquid/solid interface (Figure 1.32g). A similar study on InAs nanowires grown on (001) InAs substrate was conducted by Kang *et al.* where two similar scenarios of merging nanowires were observed despite the fact that their nanowires have different orientations compared to those in Dalacu's experiment.[124] Upon careful TEM analysis, it was found that there was a sharp transition from zinc blende to wurtzite structure at the joint region.

The ability to merge individual nanowires opens up many opportunities such as making nanoscale connections with self-aligned nanowire pairs, and is another prime example of the rich dynamic processes that can be employed in the nanowire system. With further studies to fine tune the growth dynamics this technique may be used one day to fabricate nanowire networks with higher complexity.

1.7 Summary

The field of semiconductor nanowires has seen exponential growth since the 1990s, and has impacted the development of several major fields ranging from electronics and optics to energy and biology. In this chapter we attempted to provide a basic picture of the growth mechanism and explore the different opportunities enabled by the bottom-up, additive approach. Although the basic VLS growth mechanism was presented over 50 years ago, recent discoveries on the growth dynamics have led to the development of not only atomic scale nanowires with excellent doping and morphology control but also complex nanowires structures, *e.g.*, nanowire heterostructures with clean and abrupt interfaces, branched nanowires, nanowire bridges, and complete nanowire devices, all achieved during the growth stage without complex nanofabrication techniques.

The excellent control over material composition and morphology, along with the relative ease of synthesis that allows the fabrication of large-scale, homogeneous nanowires with uniform length and diameter at defined locations, is no doubt by itself important. However, it is perhaps the ability to integrate different materials and functions in the same system with atomic precision that truly sets semiconductor nanowires apart from other nanostructures. In the next few chapters, we will see several examples of new and exciting applications enabled by this system.

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