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than the Hall mobilities obtained for much thicker (1 μm) films grown on SCAM substrates (~100 $cm^2 V^{-1} s^{-1}$).[10] We tentatively attribute this lower mobility to enhanced scattering, quantization, and/or trapping at the heterointerface. We expect that this can be overcome by separating the conduction channel from the heterointerfaces, which is feasible if ZnO/MgZnO heterointerfaces[12] are constructed on it.

In conclusion, we have studied the field-effect transfer characteristics and Hall-effect properties of lattice-matched ZnO/SCAM heterointerfaces. The carrier density deduced from Hall-effect measurements linearly increases with increasing V_G. The conductance mobility, μ, is in good agreement with the Hall mobility, indicating that the heterointerfaces are of a high quality. The field-effect mobility, μ_{FE}, increases linearly with increasing V_G and reaches values as high as 70 $cm^2 V^{-1} s^{-1}$, which is in clear contrast to the magnitude of μ_{FE} and its supralinear (exponential) V_G dependence that have been observed for polycrystalline-ZnO TFTs. From this, it can be concluded that the electronic activity of the grain boundary significantly affects the performance of ZnO-based field-effect devices.

Experimental

Thin Film Growth and Characterization: The surfaces of polished (0001) $ScAlMgO_4$ substrates were cleaved along the (0001) plane in order to obtain atomically flat surfaces over a large area (several hundred square micrometers) and to reduce the substrate thickness to approximately 100 μm. Undoped ZnO films were grown on the SCAM substrates at 700 °C by laser molecular-beam epitaxy equipped with RHEED pattern monitoring [10]. ZnO single-crystal targets were ablated using KrF-excimer laser pulses ($\lambda = 248$ nm, repetition rate = 5 Hz, laser fluence ~ 1 J cm^{-2}) in an oxygen flow of 1×10^{-6} torr (1 torr = 133.32 Pa). The thickness of the ZnO thin films were regulated during the growth by monitoring the RHEED-pattern intensity oscillations, as shown in Figure 1a. The surface morphology of the films was imaged using contact-mode atomic force microscopy in air.

Device Fabrication and Characterization: The films were patterned by photolithography and ion milling to form Hall-bars (see Fig. 1c). To ensure that the channel was fabricated in a grain-boundary-free region, the channels were positioned on areas without bunched surface steps. These steps originated from imperfect cleaving, and were seen occasionally upon inspection by an optical microscope. Ti/Au metal electrodes were evaporated onto the films and patterned by lift-off. Pt wires were placed on the electrodes using silver paste. Before polishing the back of the substrate, the sample was glued onto a glass substrate using resin. SCAM dielectric gates, approximately 10 μm thick, were reproducibly prepared by mechanical polishing and inspection by optical microscope. Finally, the gate contacts were formed on the devices mounted on tip carriers as shown in Figure 1d. The field-effect transfer characteristics and Hall-effect properties of the devices were measured at room temperature using a high-voltage gate source, and a semiconductor parameter analyzer with the electrical connections shown in the inset of Figure 3a.

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Synthesis and Fabrication of High-Performance n-Type Silicon Nanowire Transistors**

By *Gengfeng Zheng*, *Wei Lu*, *Song Jin*, and *Charles M. Lieber**

Silicon nanowires (SiNWs) are promising building blocks for the "bottom–up" approach to nanoelectronics since the physical and chemical characteristics of SiNWs, including diameter, surface composition and electronic properties, can in principle be controlled during synthesis.[1–4] To date, efforts have focused almost exclusively on studies of hole-doped or p-type SiNWs, and these materials have enabled the assembly and fabrication of field-effect transistors (FETs),[5–8] integrated logic circuits,[9] and biosensors.[10] Electron-doped or n-type SiNWs have received little attention,[5] although the in-

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trinsic electron mobility in bulk silicon is substantially larger than the intrinsic hole mobility,[11] and complementary n-type/p-type structures could be important for a number of nanoelectronic applications. A previous investigation showed that n-type SiNWs could be prepared using solid phosphorus as a dopant source in a laser-assisted catalytic growth process,[5] although the observed electron mobility values were several orders of magnitude smaller than expected for n-type silicon. Here we report the first example of controlled growth and phosphorus doping of SiNWs, and the fabrication of high-performance n-type FETs from these nanomaterials. High-resolution transmission electron microscopy (HRTEM) studies show that the phosphorous-doped SiNWs are single crystals with well-controlled diameters. Electrical transport measurements demonstrate that the doped SiNWs are n-type, although the measured transconductance values decrease with decreasing dopant concentration contrary to expectations. Four-probe measurements show that this unexpected behavior is due to dopant concentration dependent contact resistances, and yield corrected electron mobilities that depend inversely with dopant concentration as expected.

Phosphorus-doped SiNWs were synthesized using silane in a gold nanocluster mediated vapor–liquid–solid process described previously,[3,4] with phosphine as the dopant precursor. The use of gas-phase phosphorous and silicon reactants enables the phosphorus dopant concentration to be readily controlled by varying the ratio of silane and phosphine. HRTEM studies show that the SiNWs grown in this way are single crystals with diameters determined by the gold nanoclusters and have a small amount of amorphous coating (Figs. 1A, B). Images recorded close to the opposite ends of a typical 10 μm long SiNW show diameters, 22.3 and 22.7 nm, that are essentially the same. Importantly, these results demonstrate that the homogeneous deposition of Si/P does not occur during axial elongation; that is, any changes in dopant concentration will be due to variations of phosphorus concentrations incorporated via the gold nanocluster catalysts.

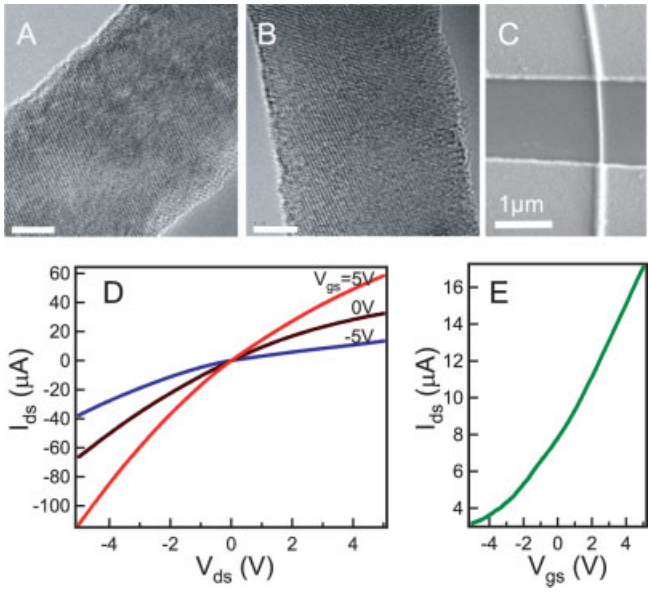

Figure 1. A,B) TEM images of two opposite ends of one 22 nm diameter n-type SiNW; the scale bar is 5 nm. C) An SEM image of a SiNW device with Ni contacts for electrical transport measurement. D) Typical I_{ds} versus V_{ds} curves of the doped (Si/P = 500) 20 nm diameter n-type SiNW device. The gate voltage for each I_{ds}–V_{ds} curve is indicated (5, 0 and –5 V). E) I_{ds} versus V_{gs} curve recorded on the same SiNW device with V_{ds} = 1 V.

To assess the electrical characteristics of these phosphorous doped SiNWs, FET devices were fabricated using standard procedures with a back gate geometry.[7–9] Figure 1D shows the current (I_{ds}) versus drain-source voltage (V_{ds}) for a typical 20 nm diameter heavily doped (Si/P reactant ratio of 500:1) SiNW. The total resistance of this SiNW device, which includes contact resistances, is ca. 80 kΩ for a gate voltage, V_{gs} = 0 V. Examination of individual I_{ds} versus V_{ds} curves shows that the current begins to saturate at positive but not negative values of V_{ds}, and that the conductance increases (decreases) as V_{gs} becomes more positive (negative). The saturation and V_{gs} are characteristic of a n-channel FET,[11,12] and thus demonstrates that the phosphorous has been incorporated as active dopant in the SiNWs. In addition, I_{ds} versus V_{gs} data (Fig. 1E) show that these 20 nm diameter n-type SiNW FETs have large on currents, which are on order of 10 μA for V_{ds} of 1 V, and relatively high transconductances of ca. 1500 nS. These on-state characteristics are attractive, although it is difficult to turn the heavily doped n-SiNWs off at values of V_{gs} smaller than the gate dielectric breakdown voltage. Measurements of the leakage current through the substrate dielectric do show that this current is much smaller (< 1 nA at –4 V) than the observed off current, and thus we suggest that this observed behavior is due to a high carrier concentration in these heavily doped materials.

We have also synthesized and characterized the electrical transport properties of SiNWs that are prepared using much lower doping levels (Si/P = 4000:1) in order to evaluate this suggestion and to further elucidate dopant concentration effects in this nanomaterial. I_{ds}–V_{ds} curves recorded with V_{gs} from –5 to 5 V (Fig. 2A) are linear for small values of V_{ds}, exhibit saturation at V_{ds} ~ 2 V, and show increases (decreases) in conductance as V_{gs} becomes more positive (negative) as expected for an n-channel FET. I_{ds}–V_{gs} data (Fig. 2B) show that the SiNW conductance changes linearly with V_{gs} in the on state with currents of several microamperes and a transconductance of 350 nS. Significantly, and in contrast to the heavily doped SiNWs, these devices can be turned off with a threshold voltage of V_{gs} ~ 0 V. The on/off current ratio determined from logarithmic plot of the data is greater than 10^4 and the subthreshold slope is ca. 300 mV/decade (Fig. 2B).

To define clearly the impact of different phosphorous doping levels, we have carried out electrical transport measurements on a large number of SiNW devices. Figure 3 shows histograms that summarize the transconductance values that are obtained for devices assembled from SiNWs synthesized using Si/P ratios of 500:1 and 4000:1. The average transconductance value for the heavily doped SiNWs (Si/P = 500:1) is 900 ± 150 nS with peak value of 2600 nS, while the average

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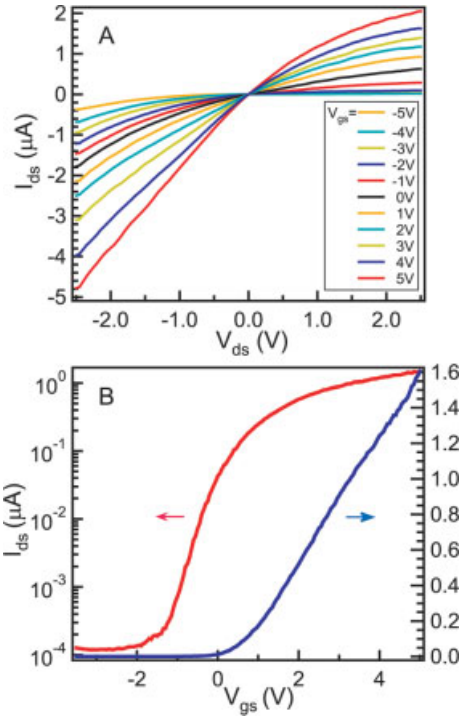

Figure 2. Electrical transport characteristics of a lightly doped (Si/P = 4000:1) 20 nm n-type SiNW device. A) I_{ds} versus V_{ds} curves recorded at different V_{gs} from –5 to +5 V. B) I_{ds} versus V_{gs} curves. The curves are displayed in linear (blue) and logarithmic scale (red), respectively and were recorded with V_{ds} = 1 V.

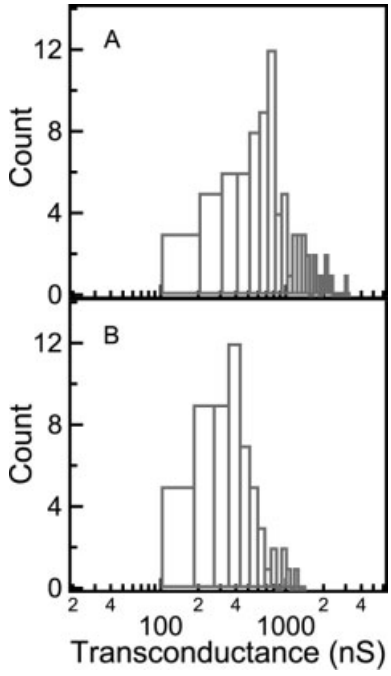

Figure 3. Histograms of transconductance values for both A) heavily doped (Si/P = 500) and B) lightly doped (Si/P = 4000) n-type SiNW device.

transconductance value for the lightly doped SiNWs (Si/P = 4000:1) is 400 ± 100 nS with peak value of 1500 nS. The average (peak) mobility values calculated[13] for the heavily and lightly doped SiNWs are 95 (270) $cm^2 V^{-1} s^{-1}$ and 50 (160) $cm^2 V^{-1} s^{-1}$, respectively.

These mobility values are more than 100 times higher than the previous work of n-type SiNW devices,[5] and suggest substantial improvement in SiNW device quality. The decrease in mobility with decreasing dopant concentration contrasts the behavior in bulk silicon, where increases in dopant concentration leads to increased scattering and a reduction in mobility.[11] While this observed dopant concentration dependent behavior in n-type SiNWs could be intrinsic to their one-dimensional geometry, we believe that the behavior is extrinsic to the nanowire and reflects the contribution from series contact resistances between the SiNWs and source/drain electrodes. Specifically, an increase in contact resistance with decreasing dopant concentration can, when comparable to the intrinsic SiNW resistance, affect significantly the measured transconductance value. The relationship between the extrinsic transconductance, g_{ex}, measured in experiments and the intrinsic transconductance g_{in} is:[12]

$$g_{ex} = \frac{g_{in}}{1+g_{in}R_s+(R_s+R_d)/R_{wire}} \quad (1)$$

where R_s and R_d represent the contact resistances of source and drain, respectfully, and R_{wire} represents the resistance of the SiNW. Hence, by determining the contact resistances, for example using four-probe transport measurements, it is possible to determine the intrinsic transconductance values.

Four-probe and two-probe transport measurements made on heavily doped (Si/P, 500:1) n-type SiNW devices (Fig. 4B)

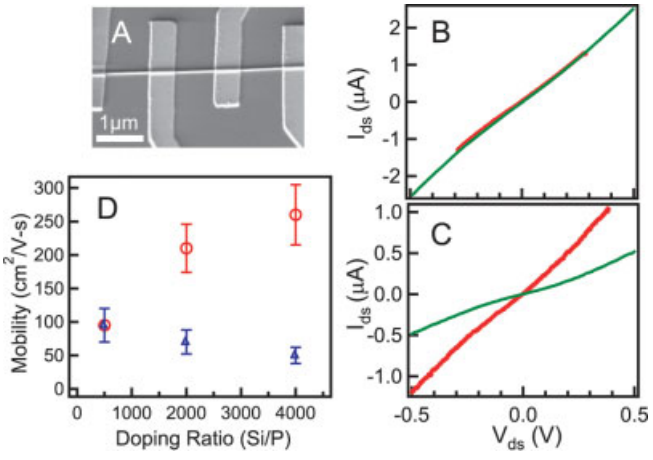

Figure 4. A) SEM image of a typical SiNW device with four contacts used for the four-probe transport measurement. B) I_{ds} versus V_{ds} data recorded on a SiNW using two-probe (green) and four-probe (red) contact geometries; the Si/P ratio was 500:1. C) I_{ds} versus V_{ds} data recorded on a SiNW using two-probe (green) and four-probe (red) contact geometries; the Si/P ratio was 4000:1. D) Measured (blue triangles) and intrinsic (red circles) mobility values, where the intrinsic values were obtained after correcting for contact resistance.

show the same I_{ds}–V_{ds} behavior, and thus show that the contact resistances are negligible in these samples. Therefore, the transconductance values measured for the heavily doped SiNW devices are essentially the same as their intrinsic values. However, transport data recorded on the lightly doped (Si/P, 4000:1) n-type SiNWs (Fig. 4C) show that contact resistance makes a substantial contribution to the measured values: the total resistance is ca. 1 MΩ, while the SiNW resistance is only 300 kΩ. Notably, the intrinsic transconductance value calculated using Equation 1 to correct for the contact resistance yields a transconductance value ca. four times larger than the measured one. We have used this approach in order to characterize a number of devices with Si/P ratios of 500:1, 2000:1, and 4000:1, and have summarized the mobility values that are obtained directly from the measured transconductances and those corrected for contact resistances in Figure 4D. We find that the average corrected mobility increases from 95 to 260 $cm^2 V^{-1} s^{-1}$ as the phosphorous doping level decreases. Significantly, this increase and the magnitude of the mobilities are in good agreement with the values reported for bulk silicon,[11] where we assume that the dopant concentration is given roughly by the reactant ratio used to synthesize the nanowires.

In summary, we have successfully synthesized single crystal n-type SiNWs with controlled phosphorus dopant concentrations for the first time. FET devices fabricated from these n-SiNWs exhibit good device properties, with mobilities more than 100 times greater than previous reports, and comparable to high-performance planar silicon FETs. In addition, four-probe transport measurements highlight the importance of contact resistance in determining the intrinsic behavior of the lightly doped nanowire devices, and thus point to an area that should benefit from future work. More generally, our advance in the growth of high-quality n-type SiNWs enables the possibility of assembling complementary n-type/p-type devices and circuits, including inverters and other logic gates, and when combined with large-scale assembly[14] and integration[15] opens up a host of opportunities in developing functional nanosystems by the bottom–up paradigm of nanoscience.

Experimental

Phosphorus-doped silicon nanowires were synthesized as follows: 20 nm gold nanocluster catalysts (Ted Pella) were dispersed on oxidized silicon substrates and then the substrates were placed in a quartz reactor. The reactor was heated to 460 °C under H_2, and then nanowire growth was carried out for 10 min by introducing silane and phosphine (1000 ppm in H_2). The total pressure was controlled at 40 torr, and the growth rate of n-type SiNWs was 0.8–1 μm min^{-1}. The phosphorus doping ratio (Si/P) was controlled by changing the ratio of flow rates of silane and phosphine. The nanowires were suspended in ethanol solution and deposited directly from solution onto TEM grids or silicon substrates for TEM and SEM imaging, respectively.

Devices were fabricated by dispersing (from ethanol solution) the n-type SiNWs onto a degenerated-doped Si substrate containing a 60 nm thick ZrO_2 dielectric layer. The source/drain contacts to the SiNWs were defined by electron beam lithography [7–9], followed by evaporation of 70 nm of Ni metal. The typical distance between source and drain electrodes was 2 μm. The devices were annealed at 380 °C for 2 min to improve the quality of Ni-Si contacts. The gate voltage was applied to the degeneratively-doped silicon substrate in a global back-gate configuration.

Four-probe transport measurements were carried out in order to determine the contact resistances. Four Ni electrodes were fabricated with 1–2 μm spacing, with the two inner electrodes serving as voltage probes and the two outer electrodes serving as current probes. The resistance of the central SiNW segment (R_{wire}) was calculated by dividing voltage over current. The two inner electrodes were also used to measure current and voltage (two-probe measurement), which provided the total resistances of the central SiNW segment and the Ni-SiNW contacts.

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